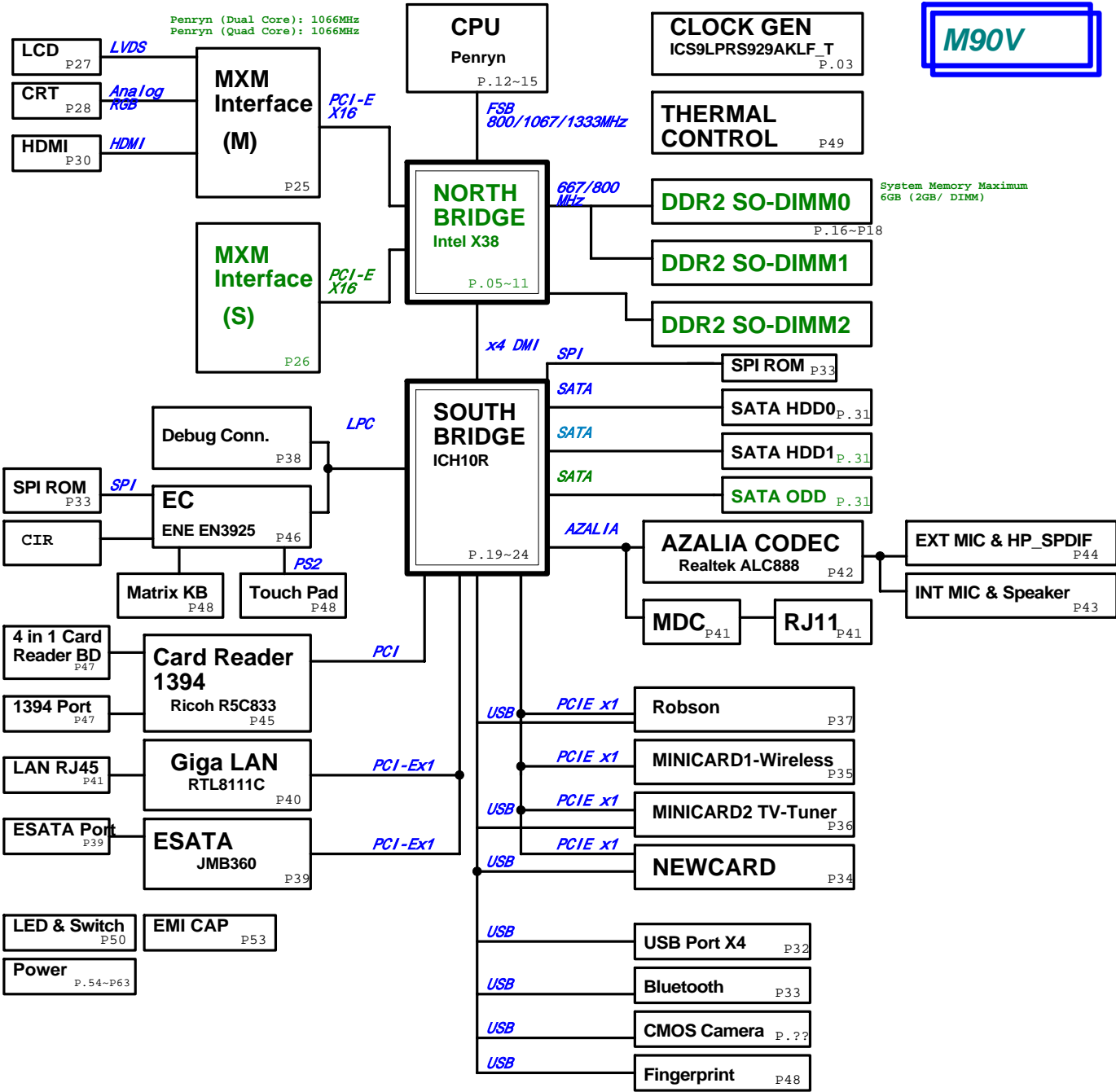
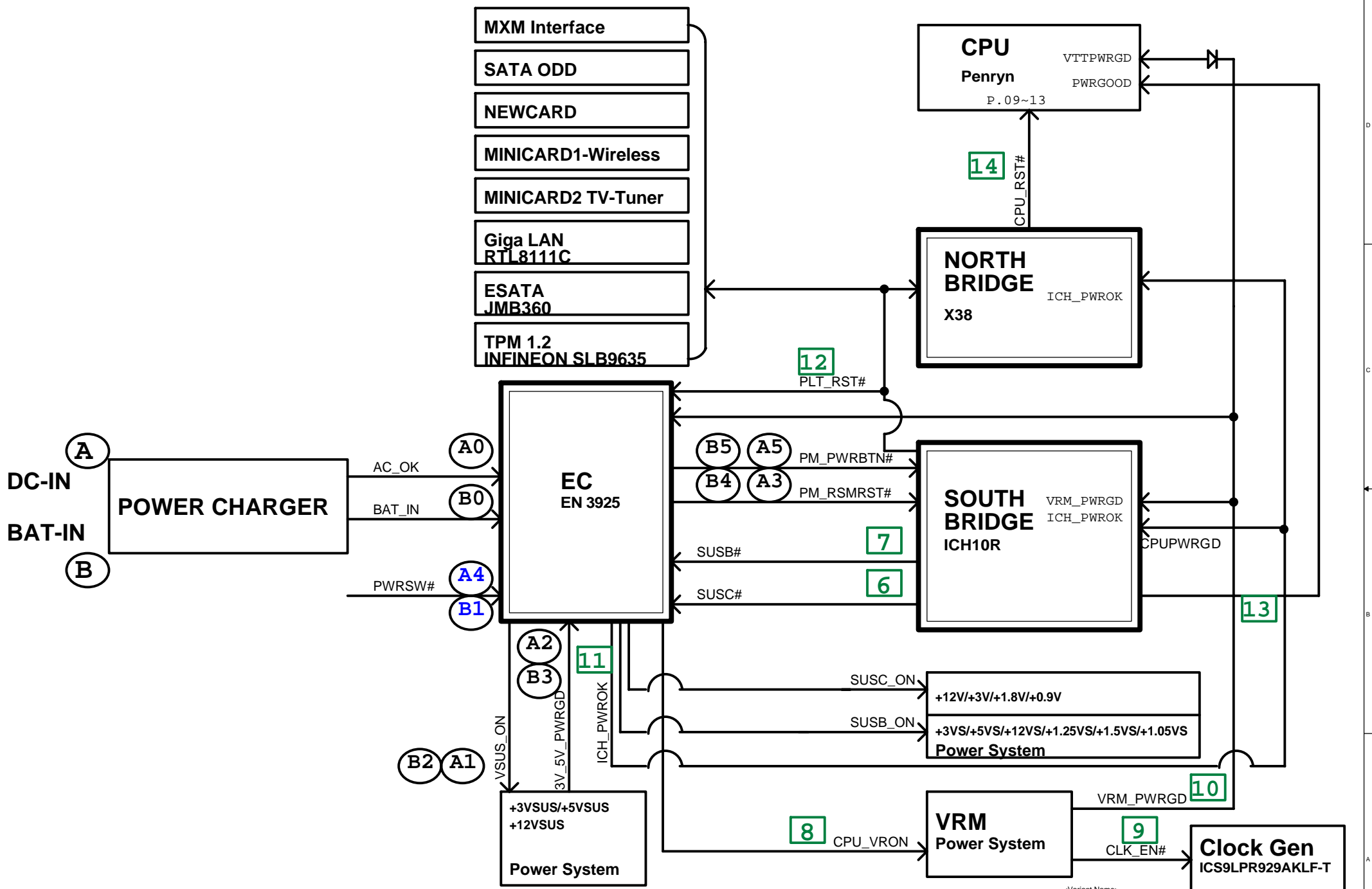
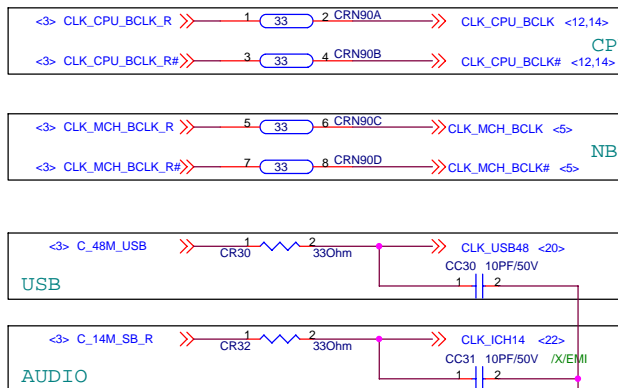
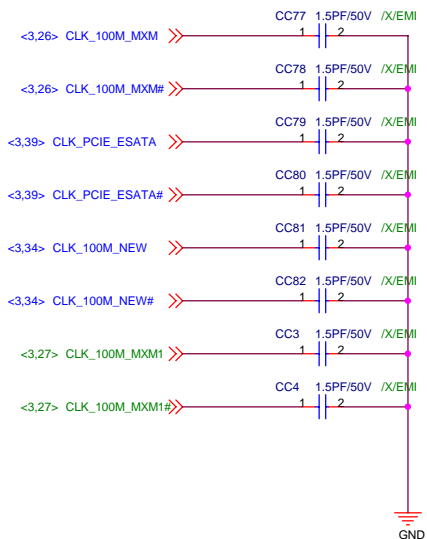


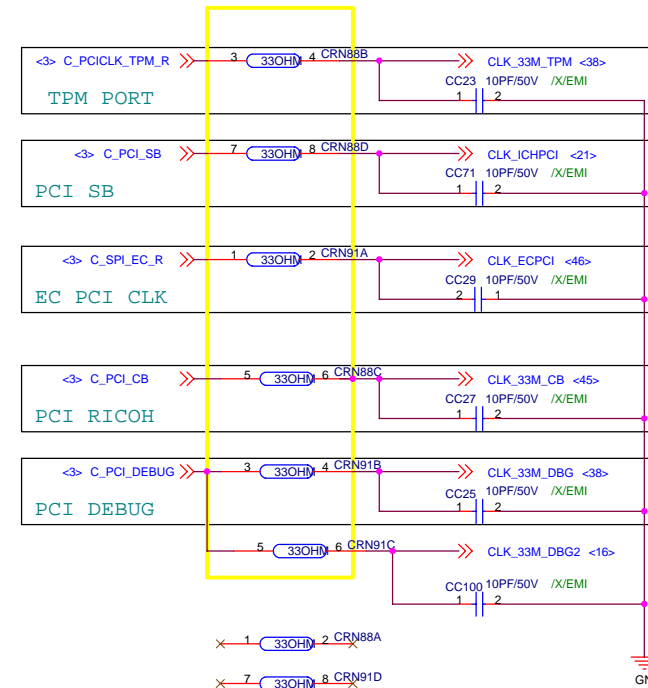
1	BLOCK Diagram
2	Power Sequence
3	Main Clock-1
4	Main Clock-2
5	BL-X CPU FSB
6	BL-X DMI / SDVO / PCIEX16
7	BL-XDDR3 CHANNEL A AND B
8	BL-X ECC / MSIC / CLINK
9	BL-X PWR CORE
10	BL-X PWR CL
11	BL-X GND/DECAPS
12	CPU-PENRYN(1)
13	CPU-PENRYN(2)
14	CPU-Capacitor
15	VID CONTROL
16	N/A
17	DDRIII_1-DIMMs
18	DDRIII_2-Termination
19	DDRIII_3-DIMMs
20	ICH9 DMI / USB / PCIExpress
21	ICH9 PCI / LAN / SPI / RTC
22	ICH9 LPC / SMBUS / HD / MISC
23	ICH9 CLINK / SATA / FAN /CPU
24	ICH9 POWER
25	ICH9 GND
26	MXM1 Interface
27	MXM2 Interface
28	NBIO_1-LVDS & Inverter
29	NBIO_2-CRT
30	NBIO_3-HDMI Connector
31	SBIO_1-SATA_HDD & IDE_ODD
32	SBIO_2-USB & DAUGHTER
33	SBIO_3-BlueTooth & SPI
34	SBIO_4-EXPRESS CARD
35	SBIO_5-Mini Card1-Wireless
36	SBIO_6-Mini Card2-MINICARD
37	SBIO_7-TPM/Debug/I2C_GPIO
38	JMB363-1
39	JMB363-2
40	PCIE-GLAN-Marvell 88E8056
41	MDC&RJ45/RJ11
42	Audio_1-Realtek ALC883
43	Audio_2-Speaker / MicA
44	Audio_3-Phone Jack
45	PCI-Reader-R5C833
46	EC ENE3925
47	PCI-Reader-Connector
48	ECIO_1-ISA ROM & KB & TP
49	ECIO_2-FAN
50	LED & SW
51	DC IN & BAT IN & Discharge
52	Screw Hole & Nut
53	EMI CAP
54	POWER_VCORE
55	POWER_SYSTEM
56	POWER_1.5VS & 1.05VS
57	DDR3 POWER (1.5V)
58	MXM POWER (1.8V)
59	NB POWER (1.25V)
60	POWER I/O +3VA
61	POWER CHARGER
62	POWER LOAD SWITCH
63	POWER GOOD DETECTER
64	HISTORY
65	POWER SEQUENCE



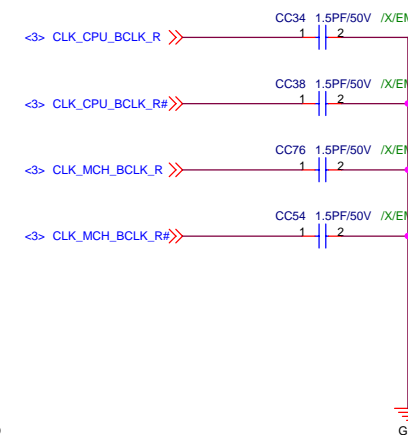
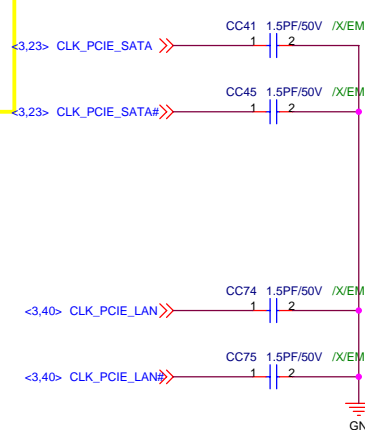
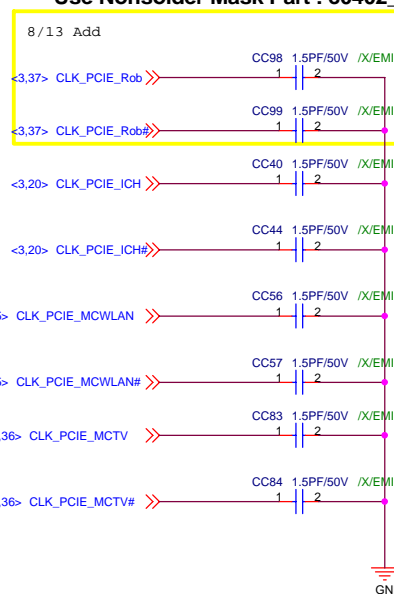
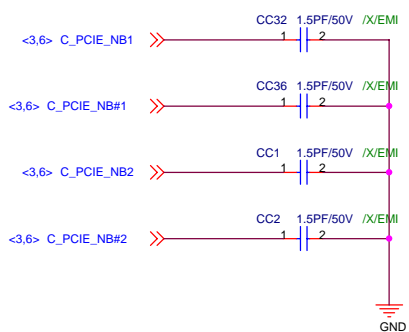




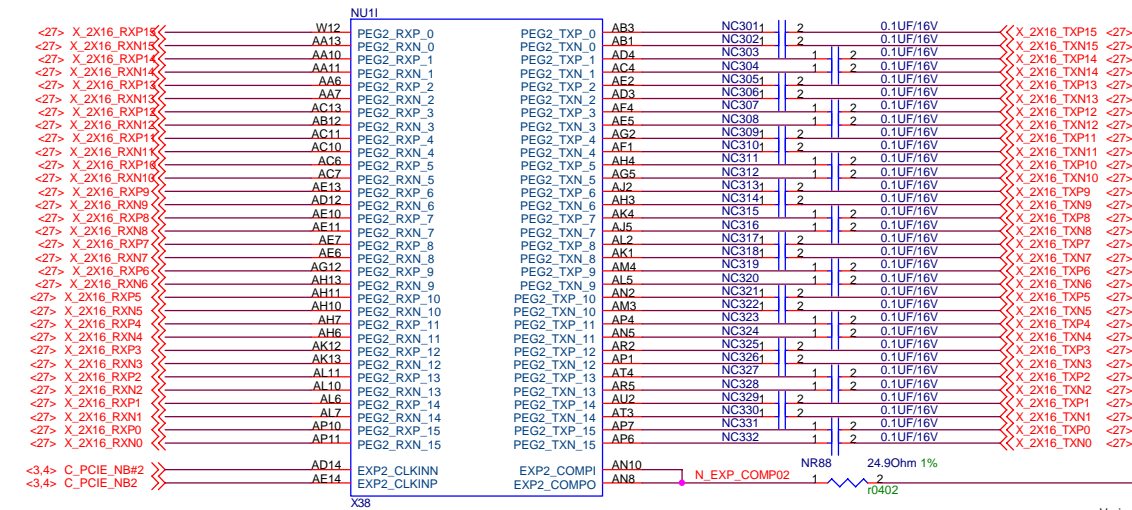
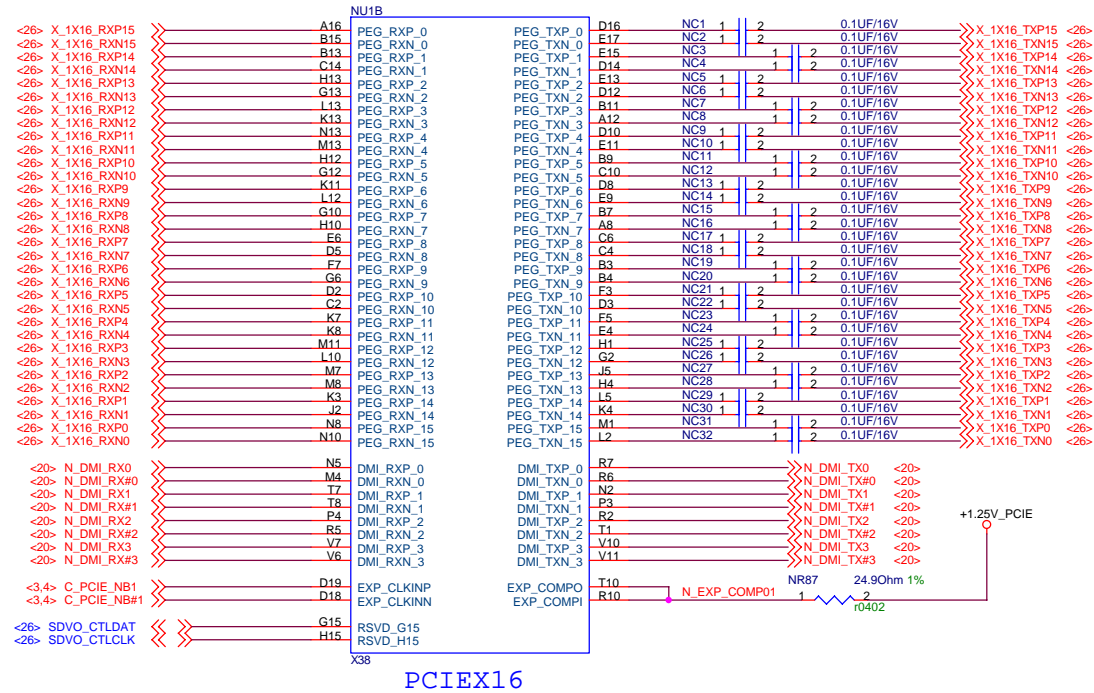
del. DOT 96M



Place them closed to Destination for Measurement
Use Nonsolder Mask Part : c0402_nomask

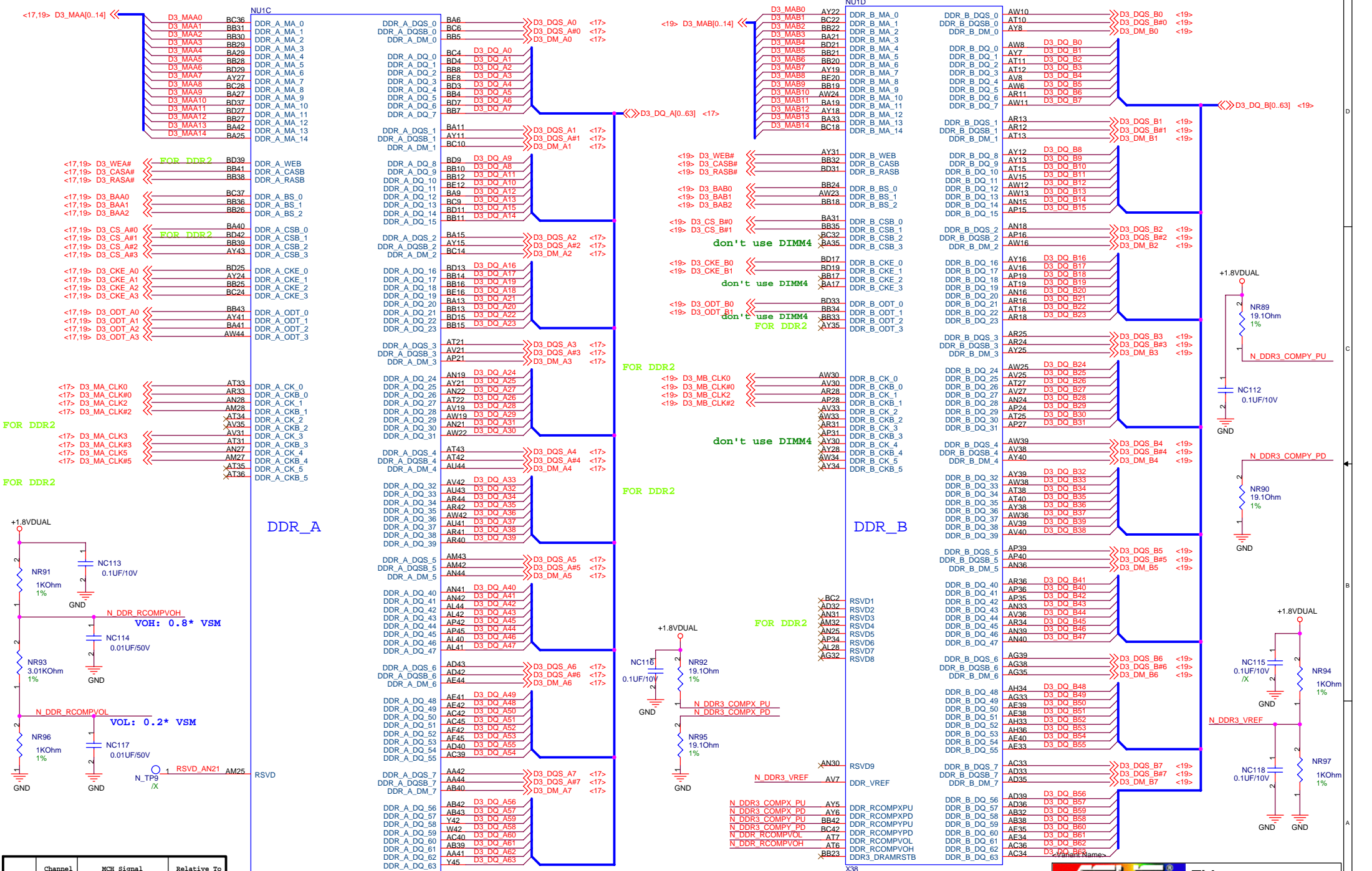


<Variant Name>			
		Title : Main Clock-2	
ASUSTek Computer Inc.		Engineer: Tony Kao	
Size A3	Project Name M90V		Rev 2.0
Date: Wednesday, June 18, 2008		Sheet	4 of 65



<Variant Name>

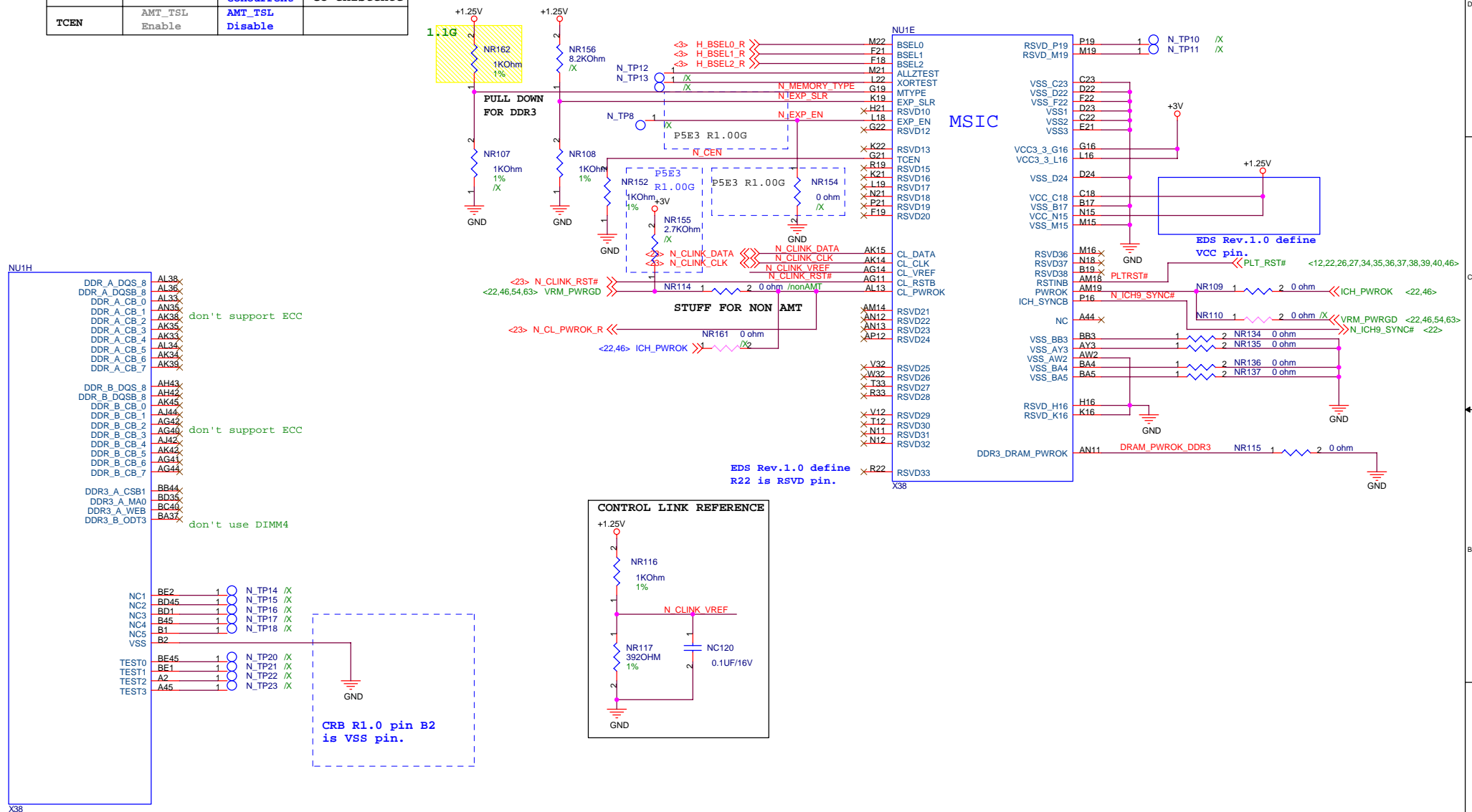
ASUS		Title : BEARLAKE-X-2	
ASUSTek Computer Inc.		Engineer: Rex Chang	
Size	Project Name	Rev	
A3	M90V	2.0G	
Date: Wednesday, June 18, 2008		Sheet	6 of 65

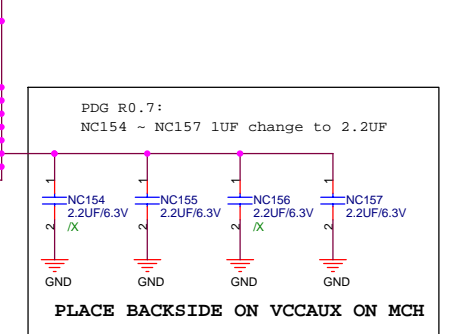
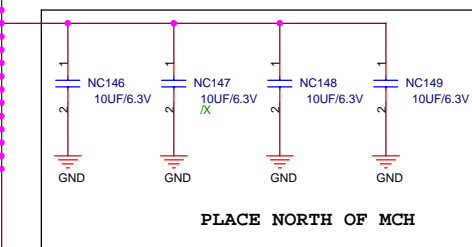
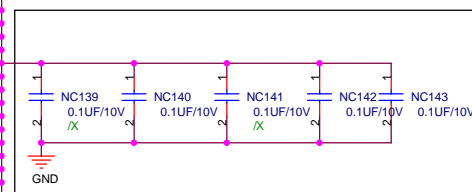
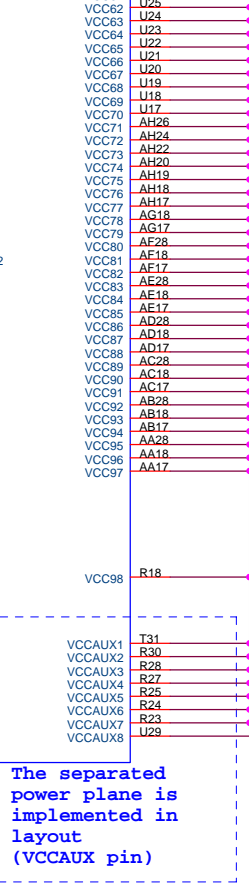
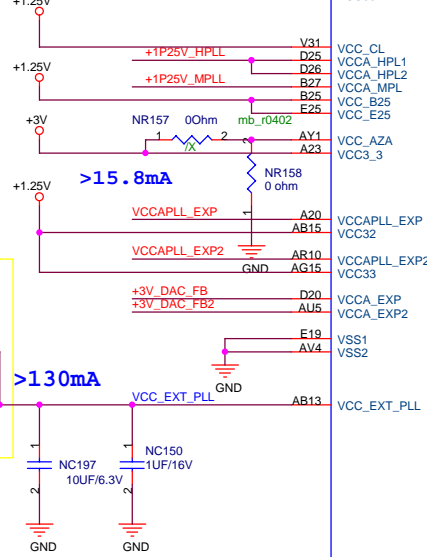
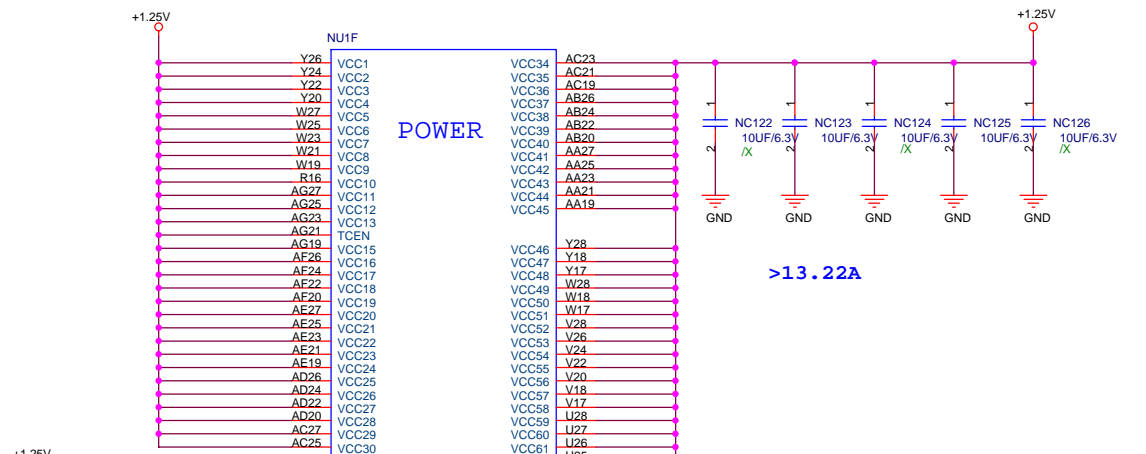
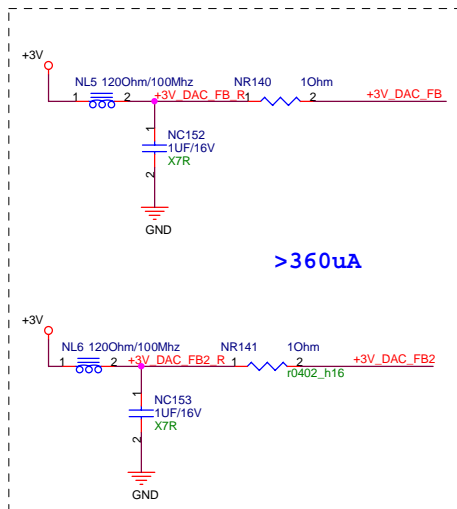
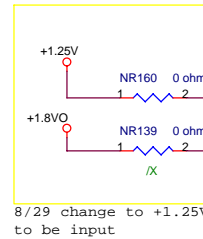
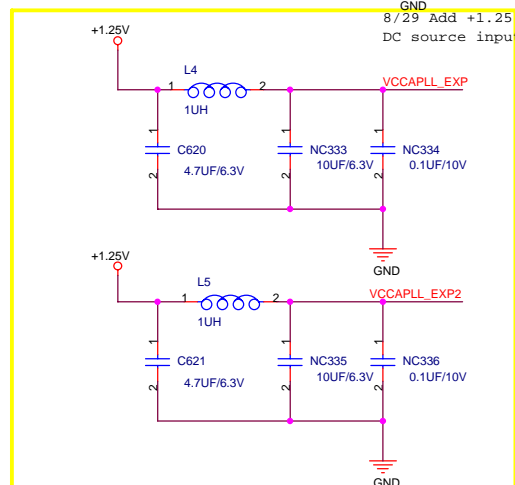
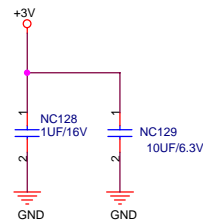
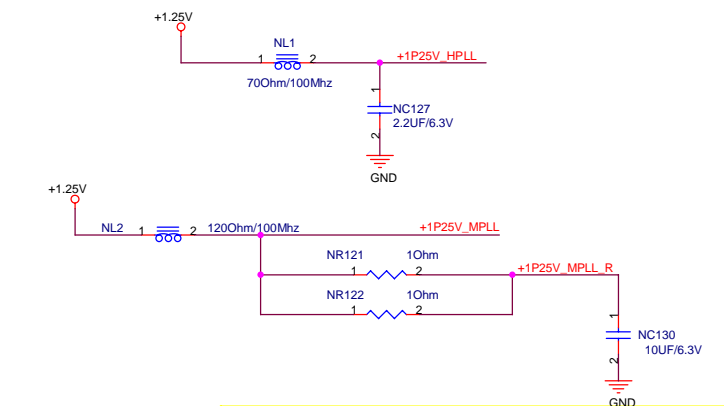


Channel	MCH Signal		Relative To
	DDR A CK/ CKB[2 & 0]	DDR A CK/ CKB[3 & 5]	
A	DDR A CK/ CKB[1 & 4]	No connect	DIMM0
	DDR B CK/ CKB[2 & 0]	DDR B CK/ CKB[3 & 4]	
B	DDR B CK/ CKB[1 & 5]	No connect	DIMM1
	DDR A CK/ CKB[2 & 0]	DDR A CK/ CKB[3 & 4]	

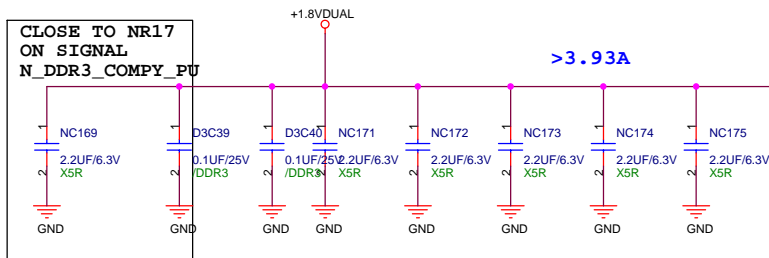
Net Name	H	L	Description
MTYPE	DDR2	DDR3	Memory Type select
EXP_SLR	Norm (For)	Reverse (For uBTX)	PCI-E LANE Reversal
EXP_EN	ATX Concurrent	Non-Concurrent	PCI-E / SDVO Co-existence
TCEN	AMT_TSL Enable	AMT_TSL Disable	

MCH BSEL TABLE			
BSEL2	BSEL1	BSEL0	FSB Frequency
0	0	0	267MHz (1067)
0	1	0	200MHz (800)
1	0	0	333MHz (1333)

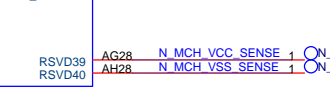
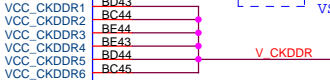
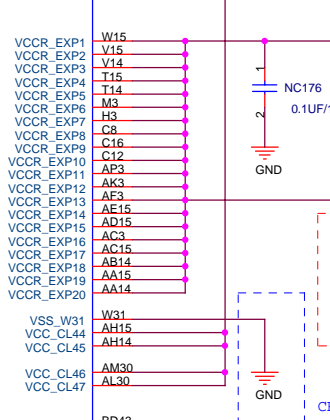
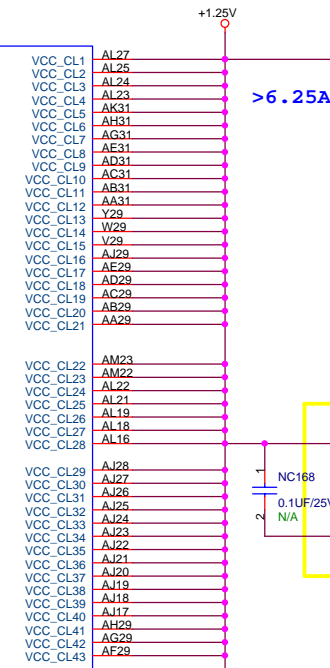
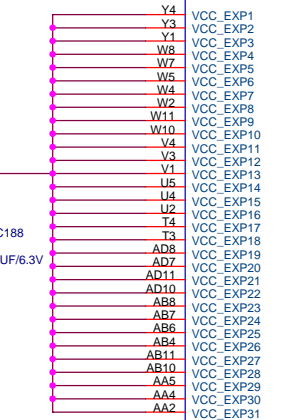
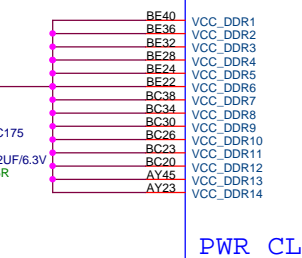
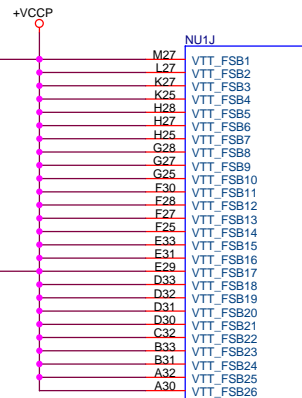
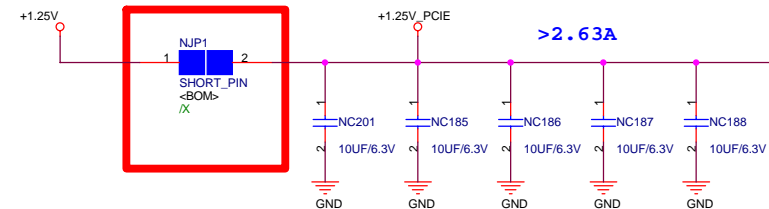




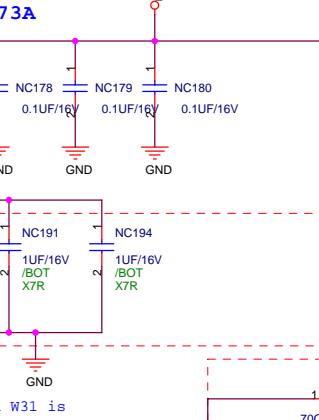
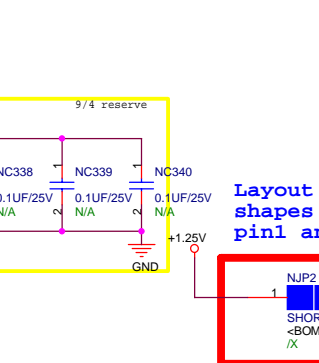
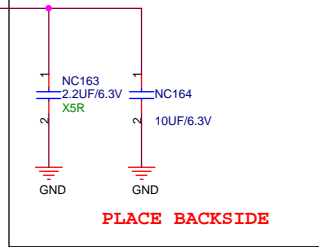
CLOSE TO NR17
ON SIGNAL
N_DDR3_COMPY_PU



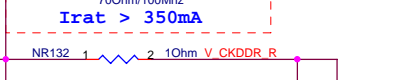
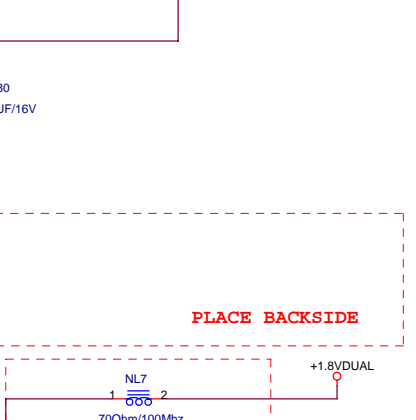
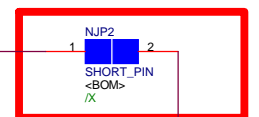
Layout used big
shapes cover NJP1
pin1 and pin2

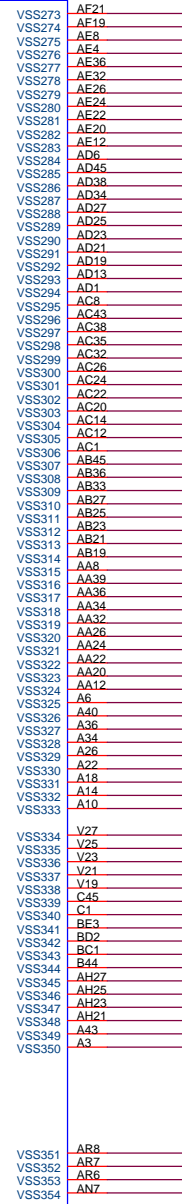
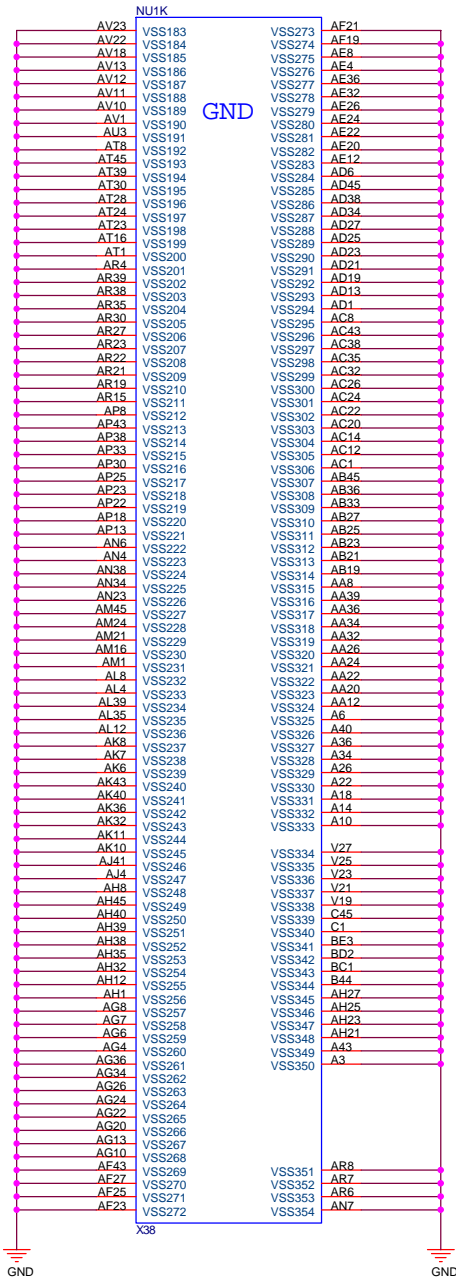
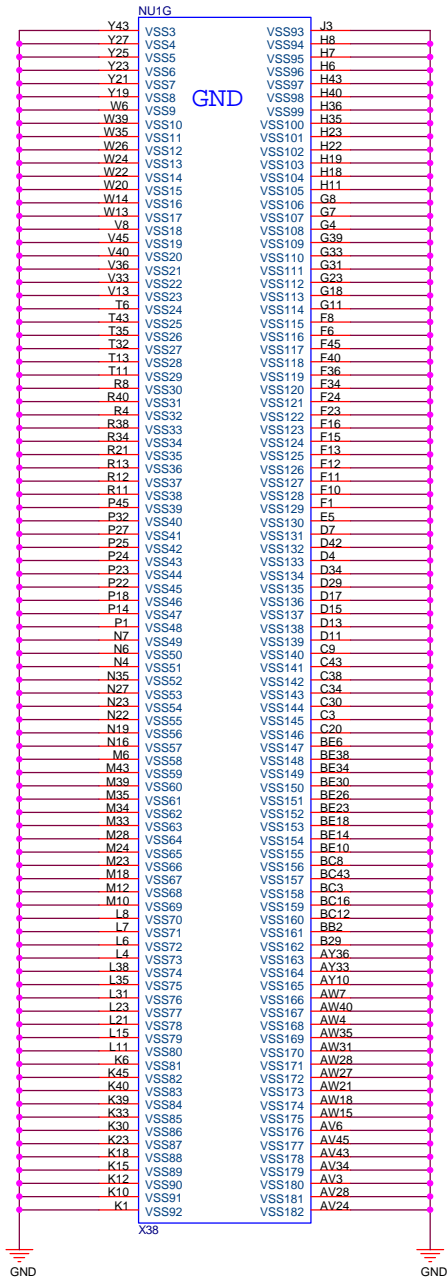


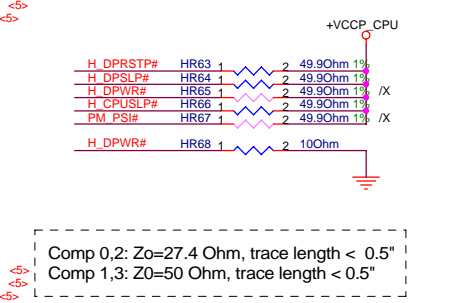
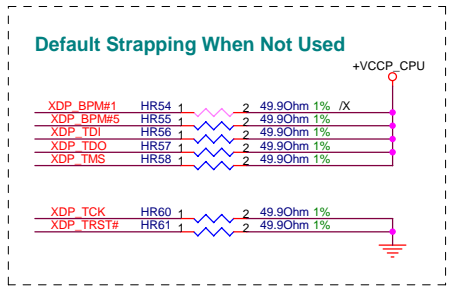
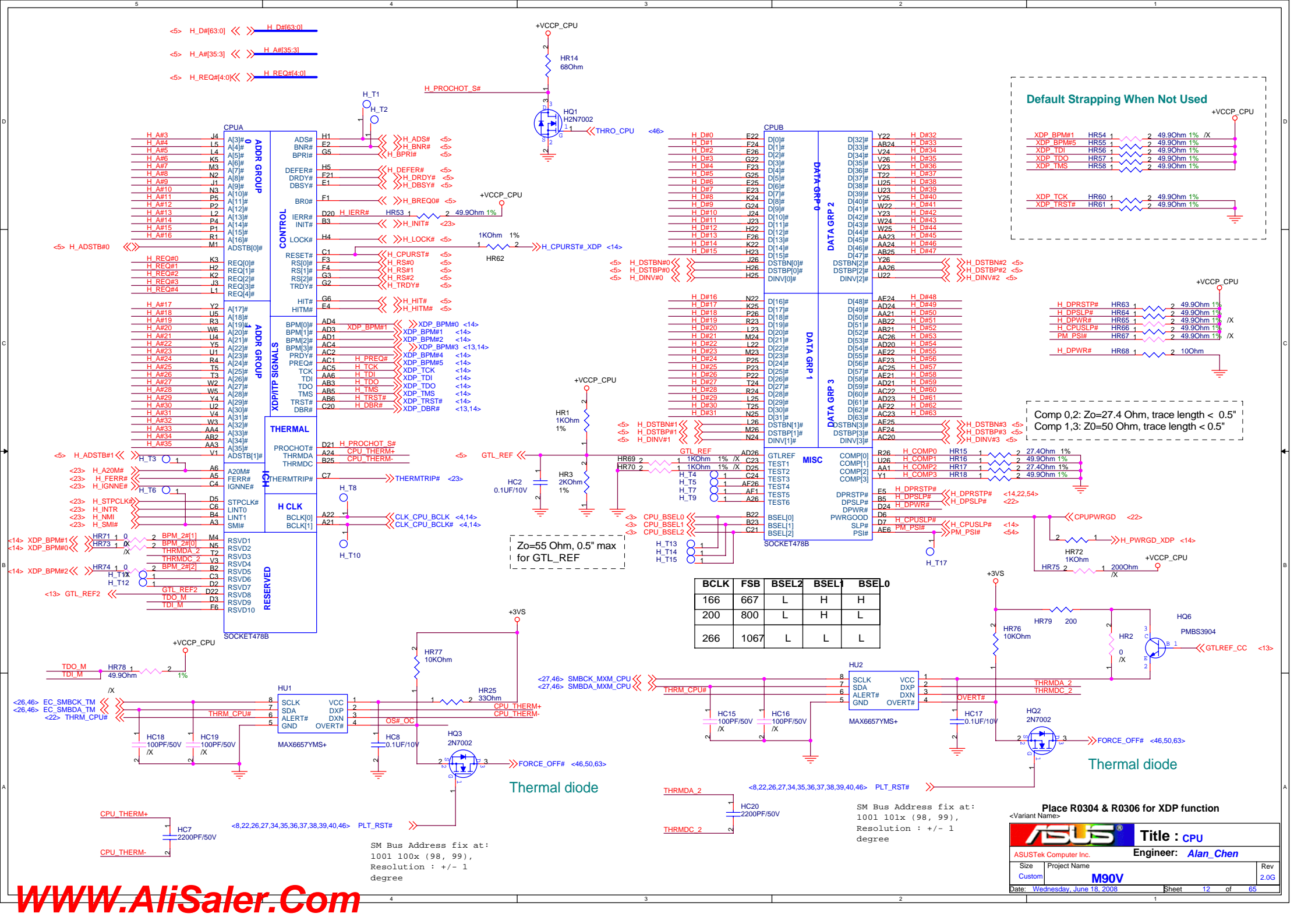
MOW WW50_2006:
Intel's platform power-delivery
simulation analysis has resulted
in the removal of back-side
decoupling caps for VCC_Core.



Layout used big
shapes cover NJP2
pin1 and pin2







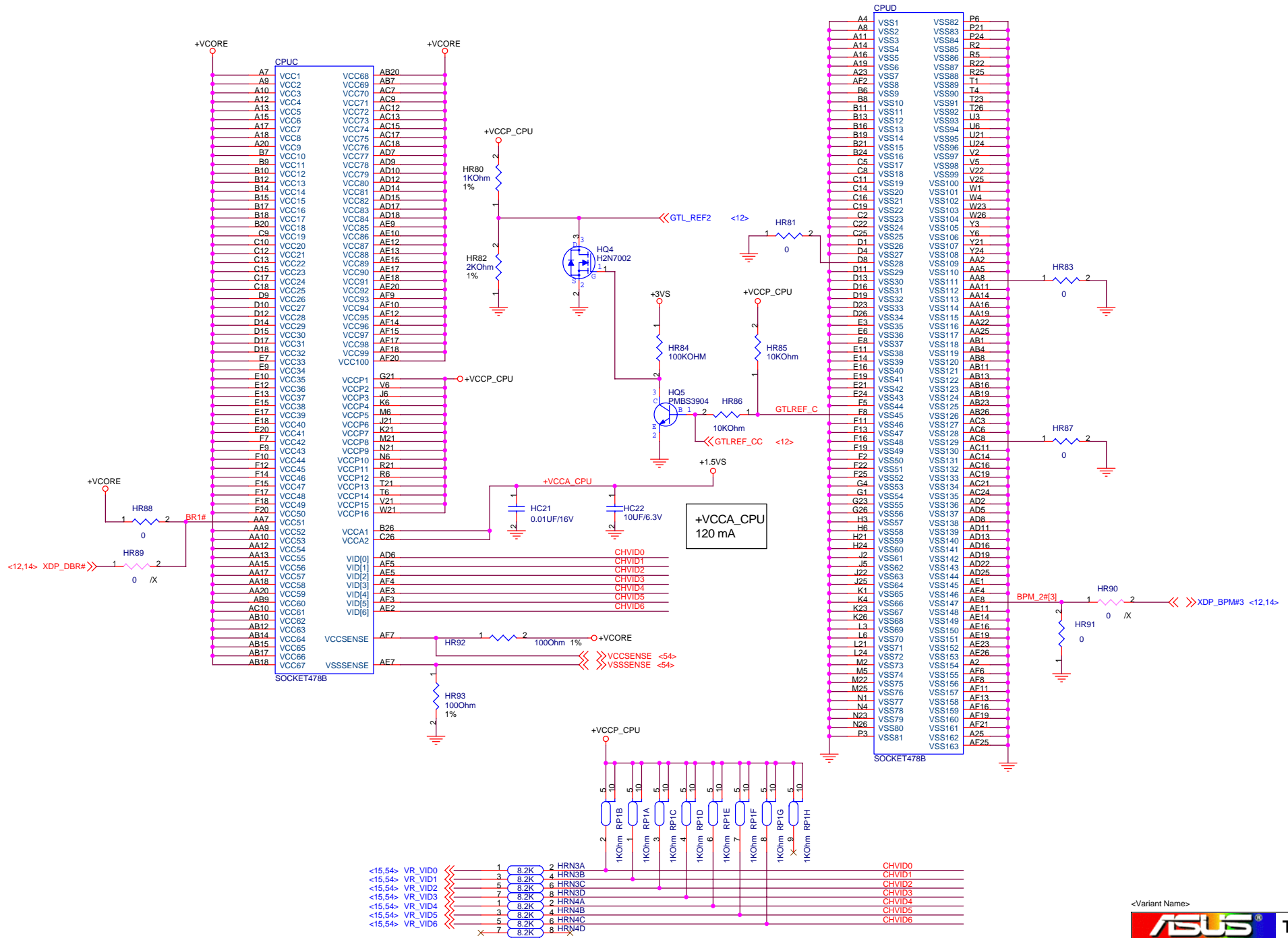
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

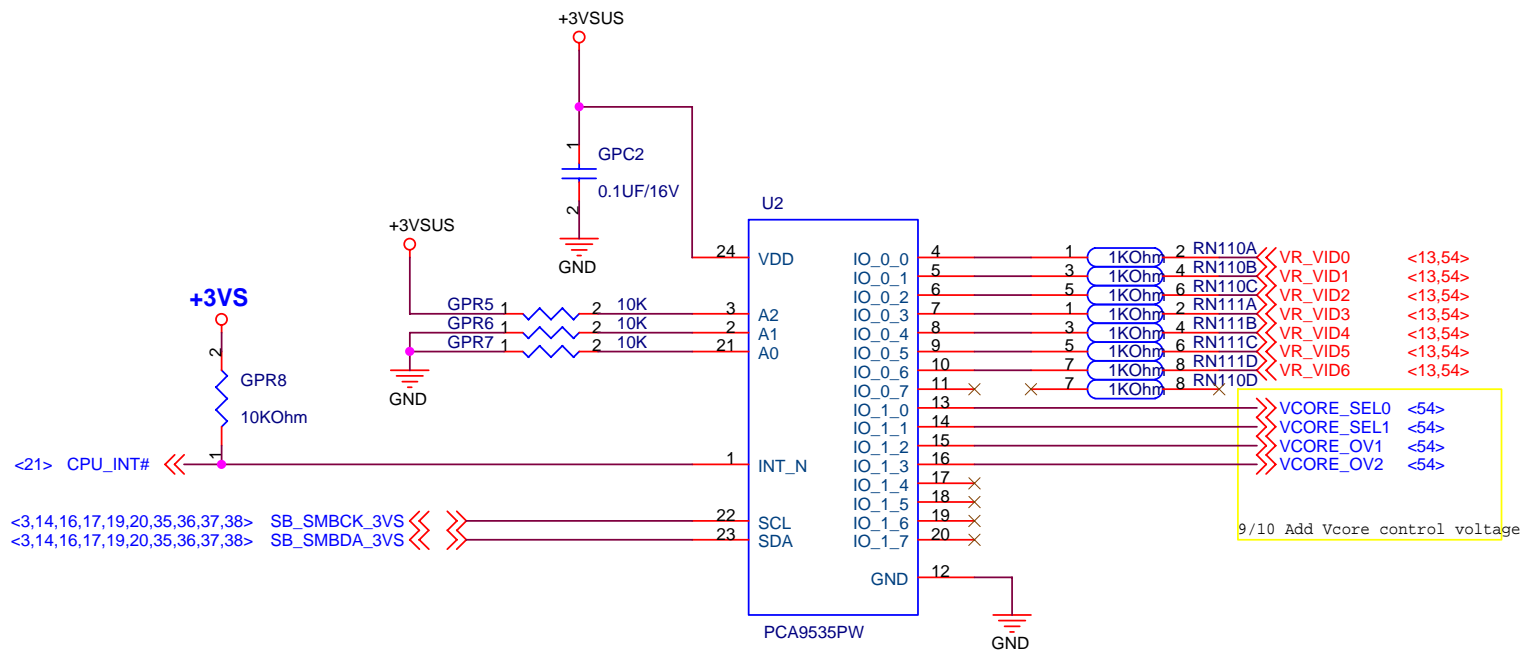
ASUS Title: CPU

ASUSTek Computer Inc. Engineer: Alan Chen

Size Project Name M90V Rev 2.0G

Date: Wednesday, June 18, 2008 Sheet 12 of 65

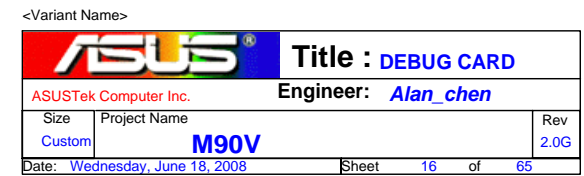


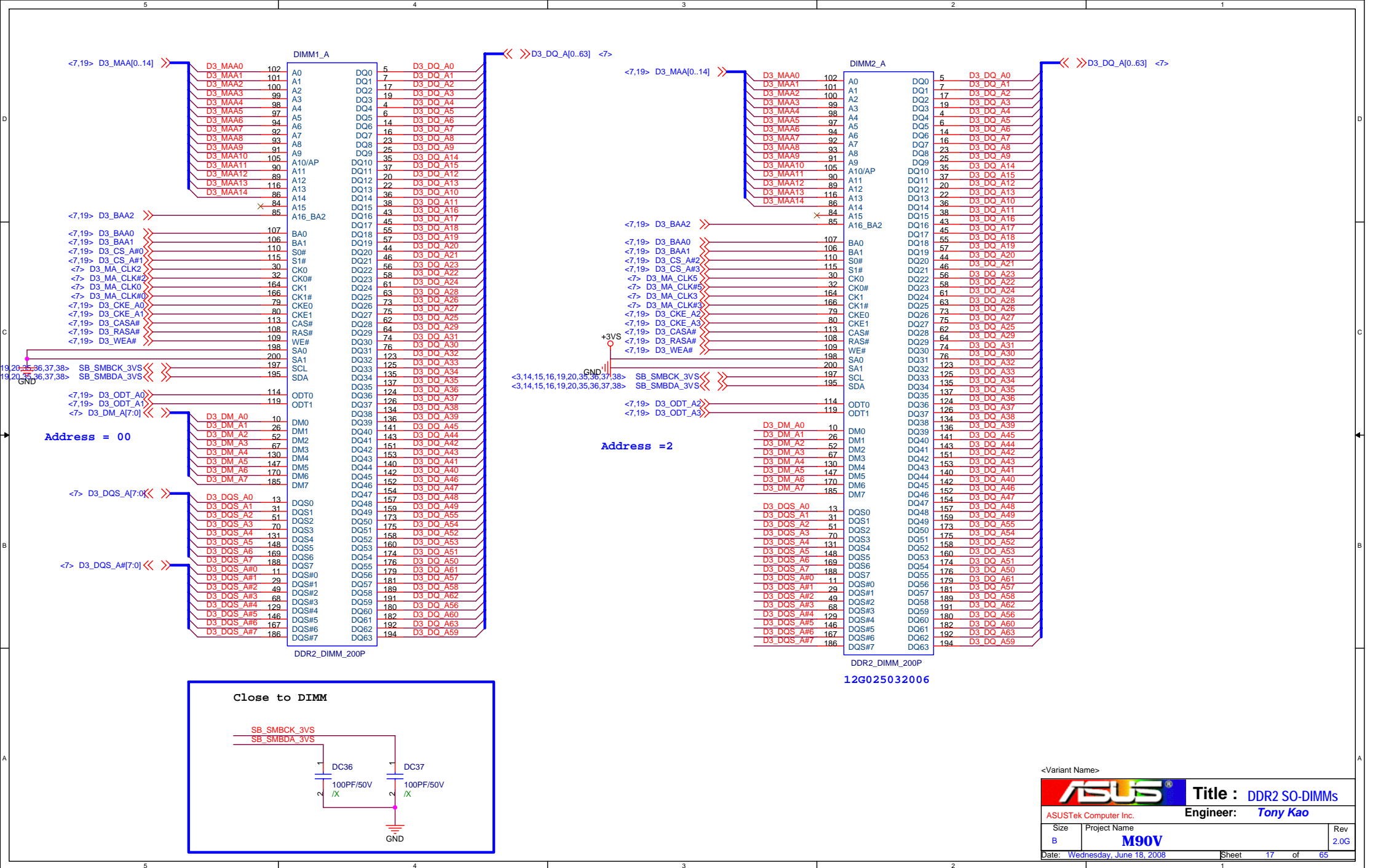


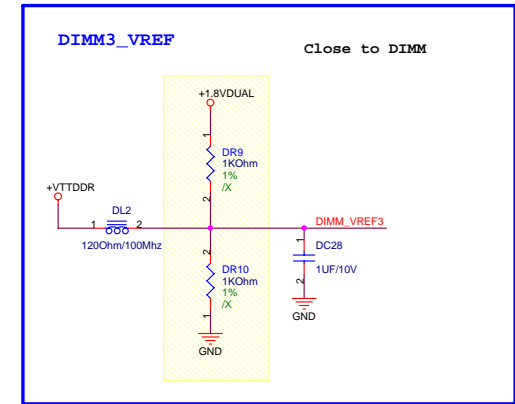
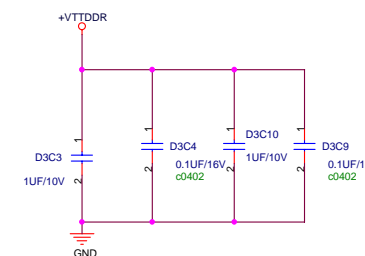
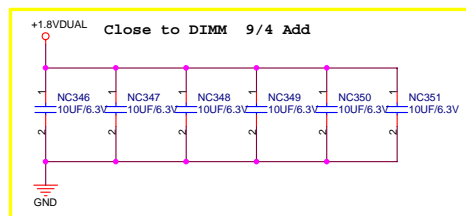
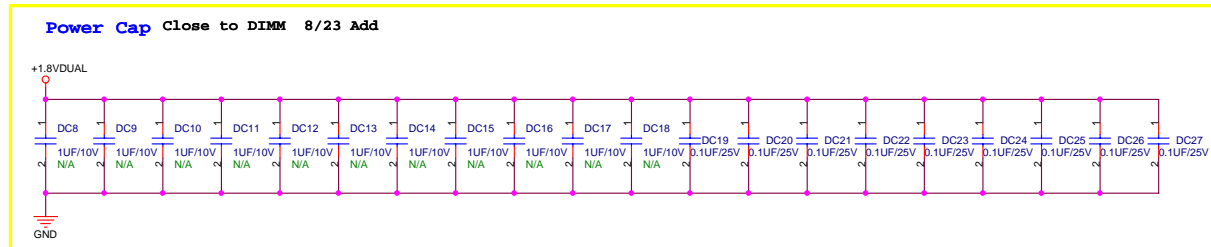
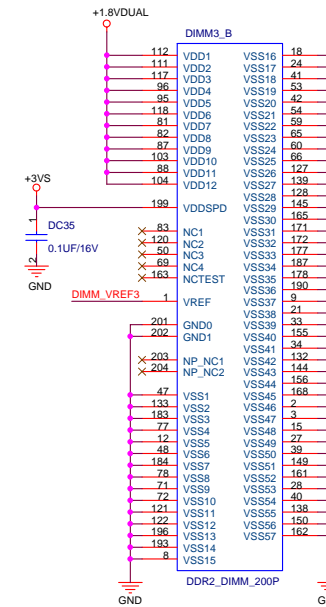
<Variant Name>

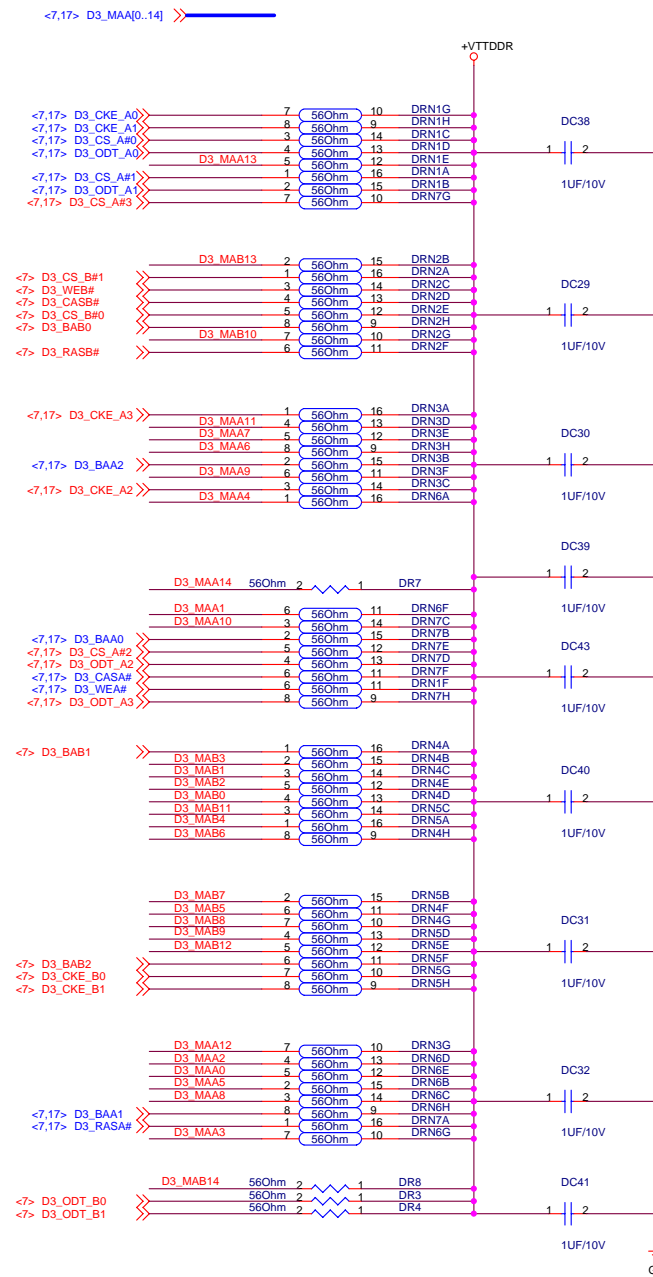
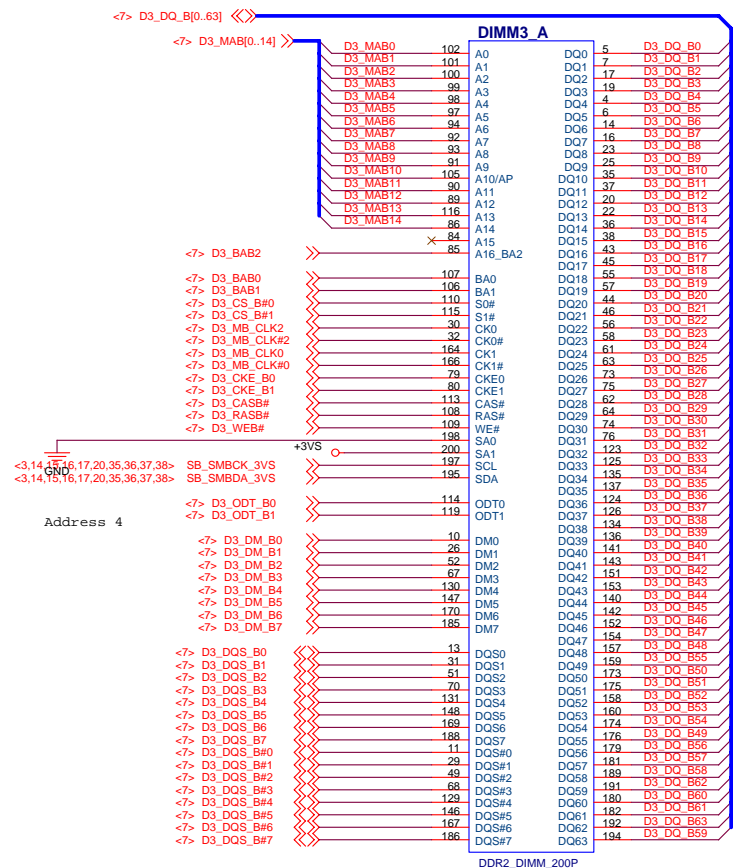
ASUS		Title : vid	
ASUSTek Computer Inc.		Engineer: Rex Chang	
Size A4	Project Name M90V		Rev 2.0G
Date: Wednesday, June 18, 2008		Sheet	15 of 65

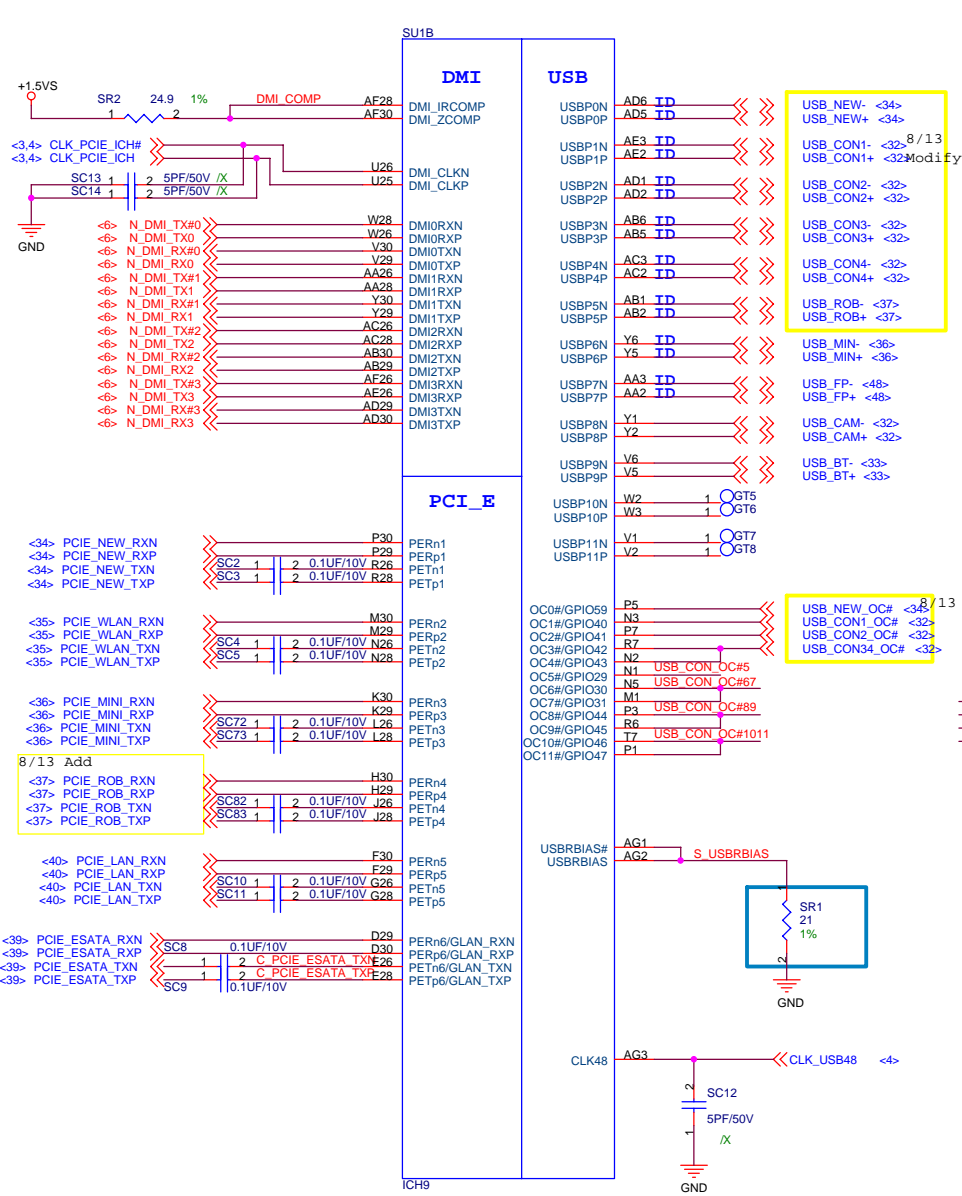
Block C



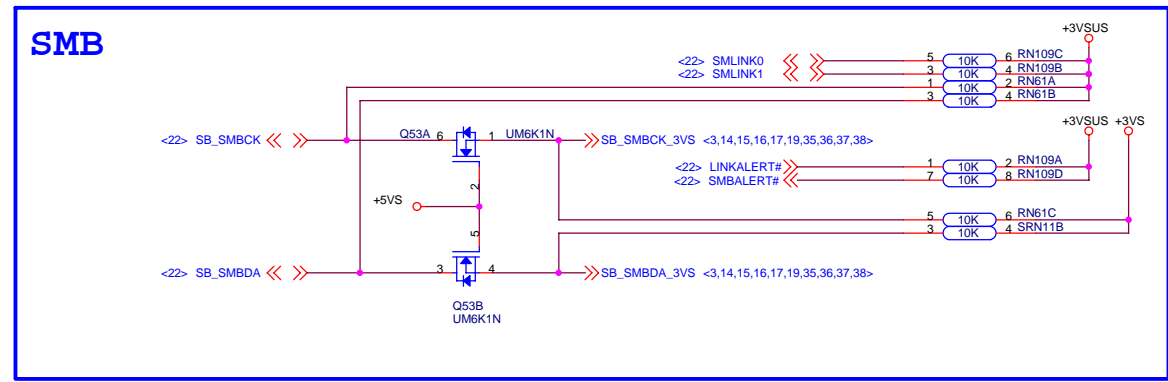
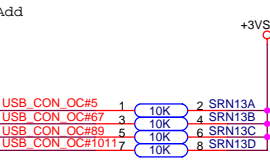


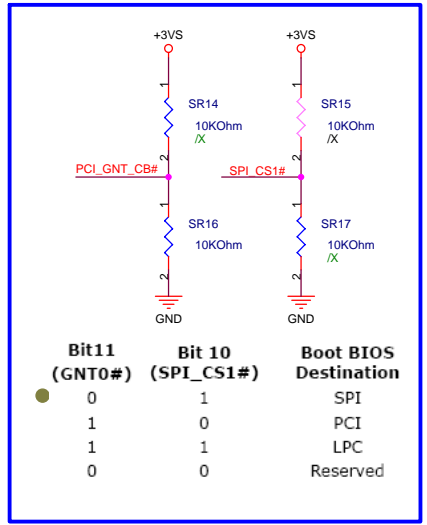
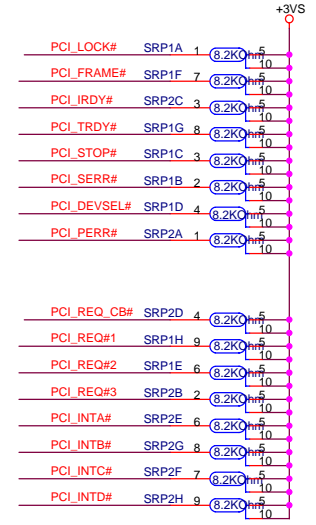
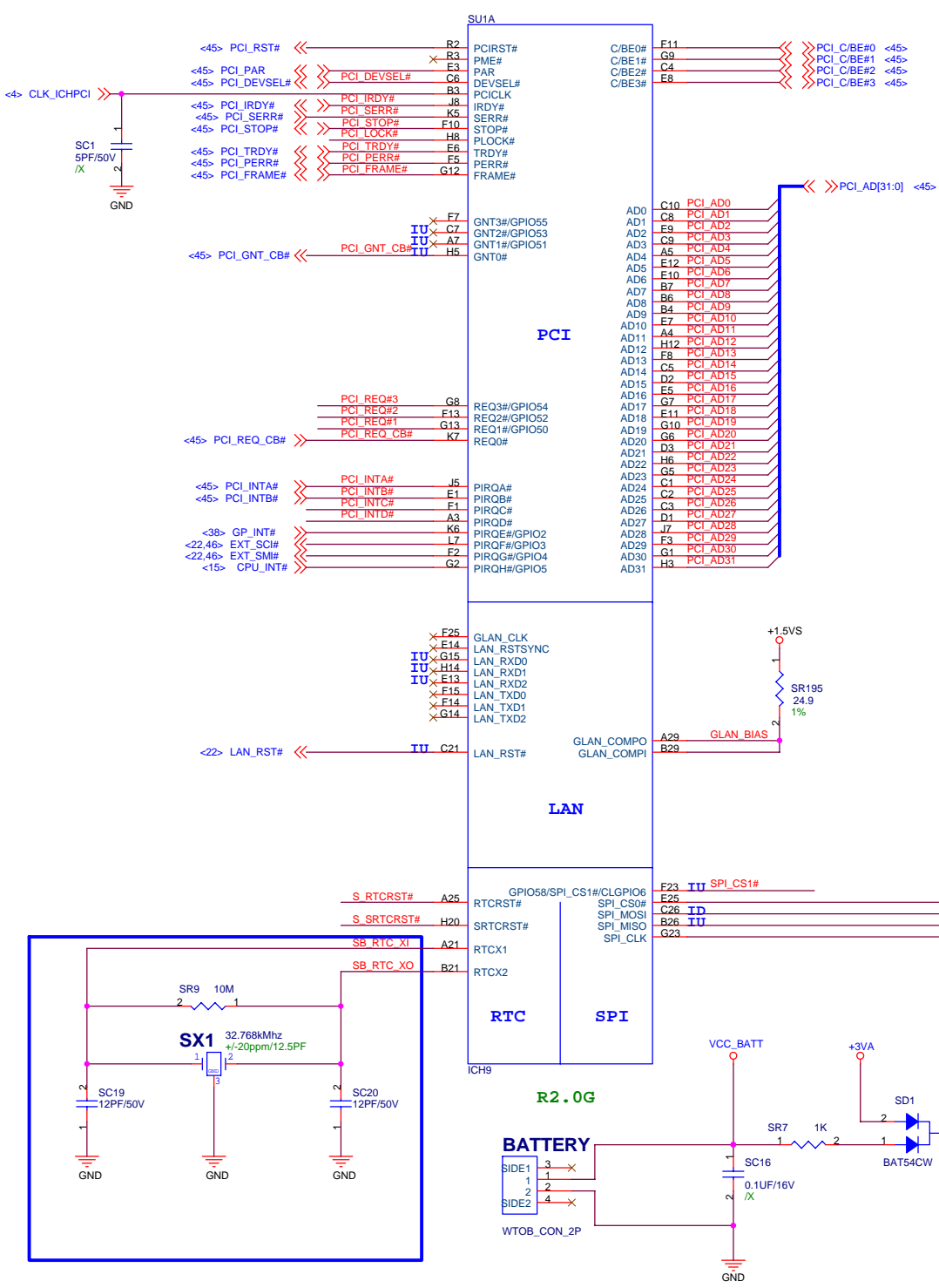


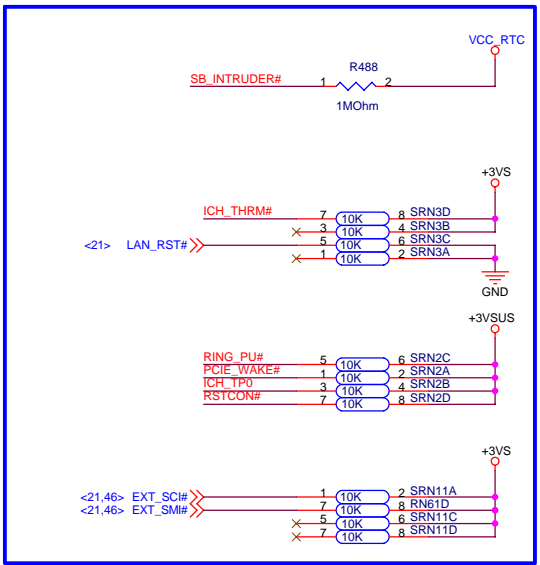




USB 0	USB NEW
USB 1	USB Conn.
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB Conn.
USB 5	Robson
USB 6	USB Mini
USB 7	USB FP
USB 8	USB Cam
USB 9	USB BT







Straping Pin

No Reboot

ICH_SPKR SR198 10K

Flash Descriptor Security Override

GPI033 SR199 10K

DMI Termination Voltage: GPIO49 internal pull up 20K

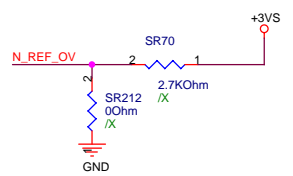
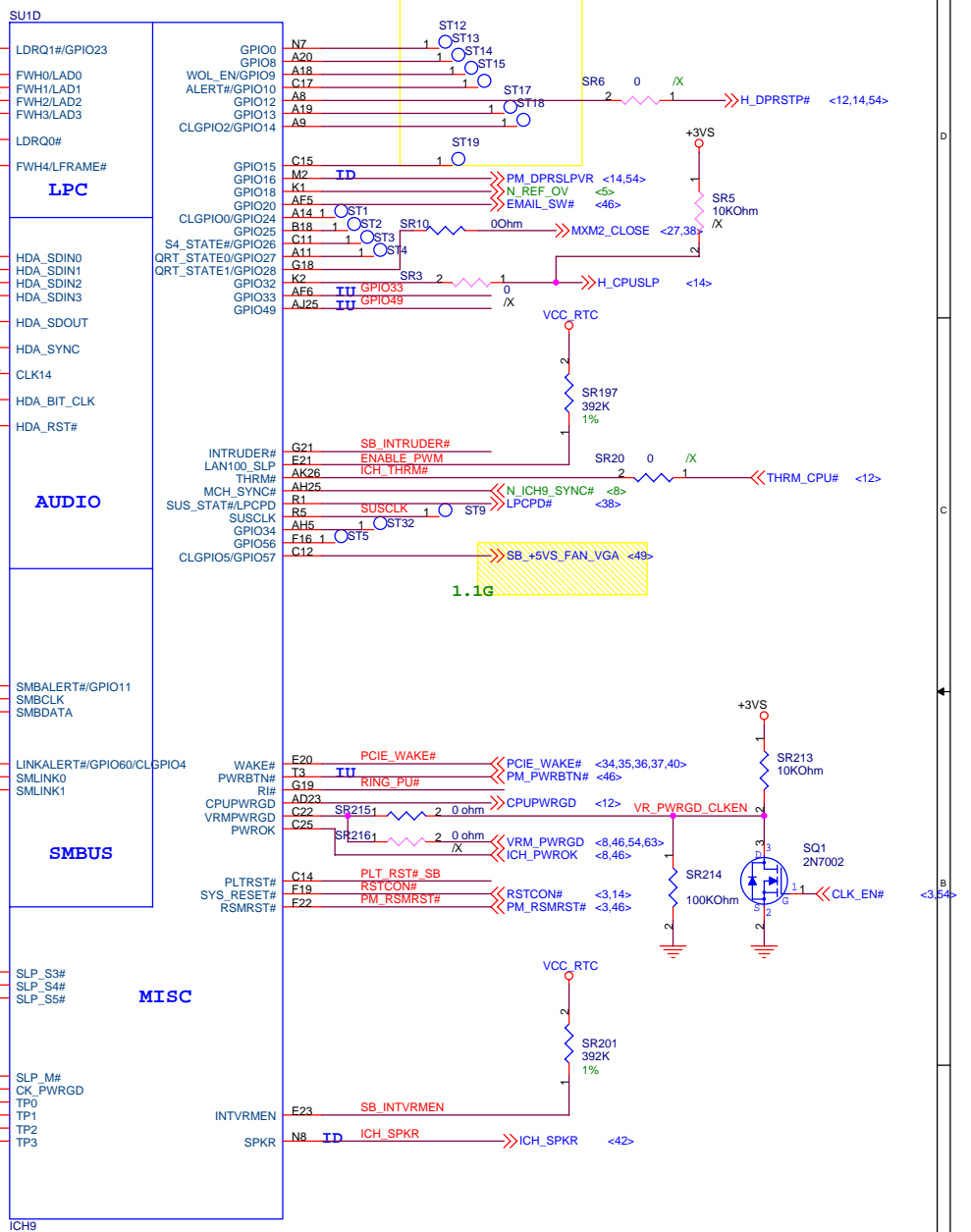
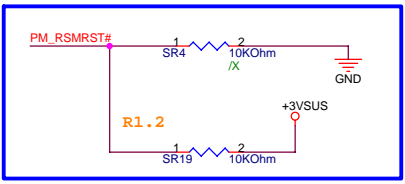
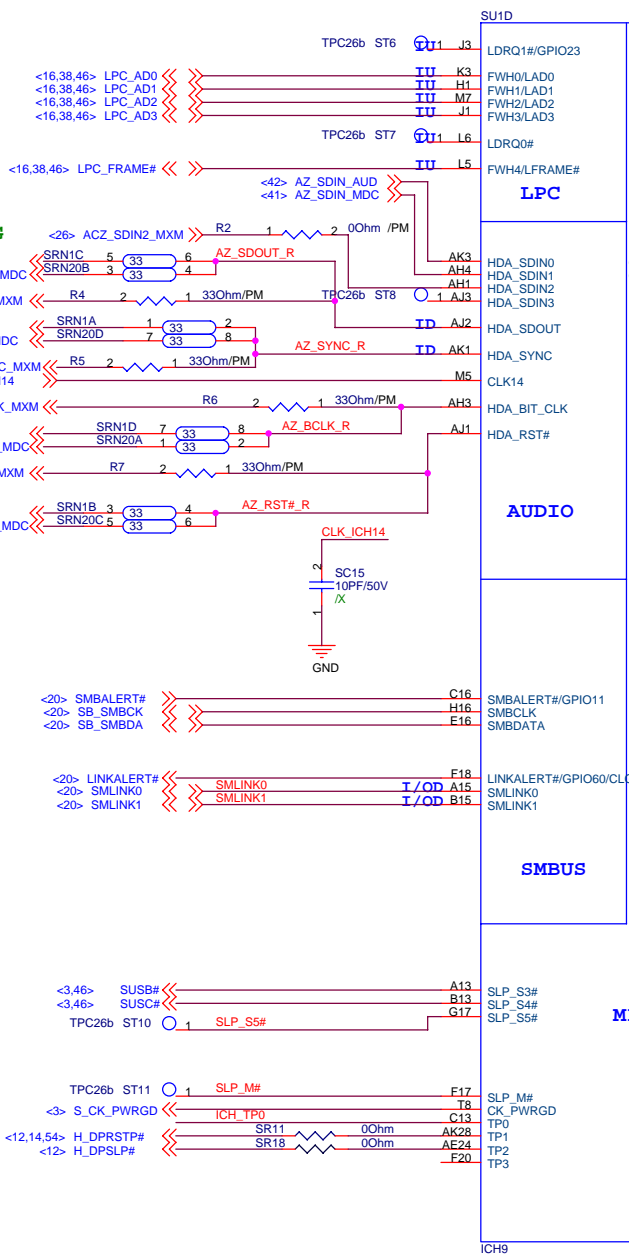
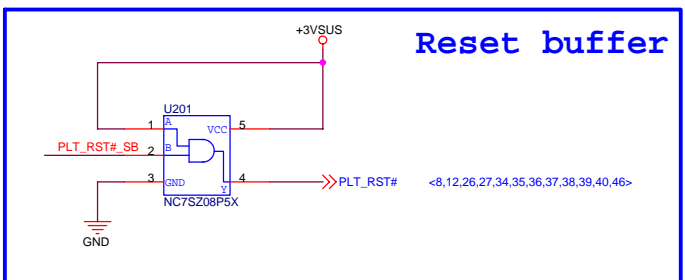
GPI049 SR200 1K

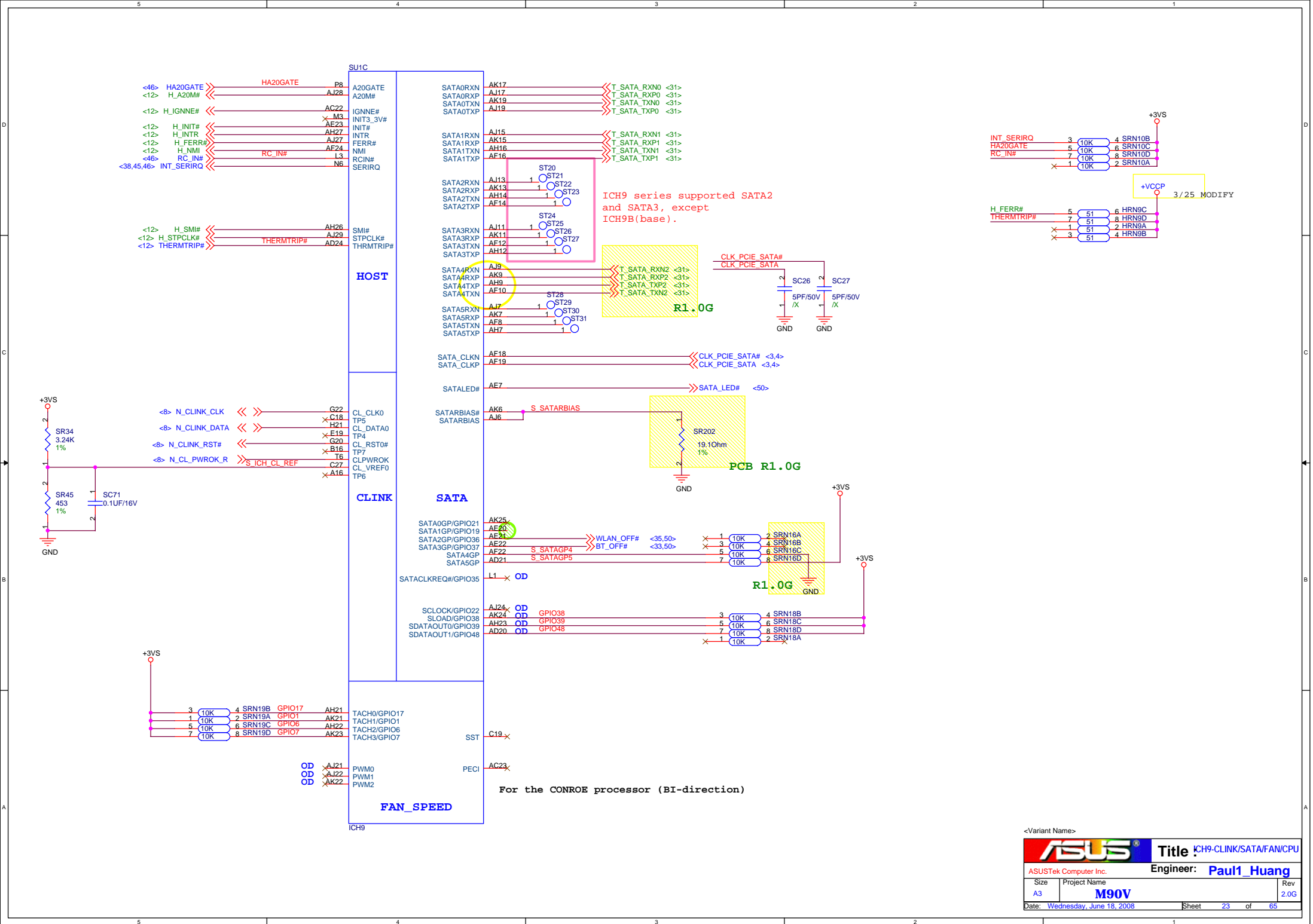
PCIE Port Config.

AZ_SDOUT_R SRN15A 2 100K
 AZ_SYNC_R SRN15D 8 100K
 SRN15C 6 100K
 SRN15B 4 100K

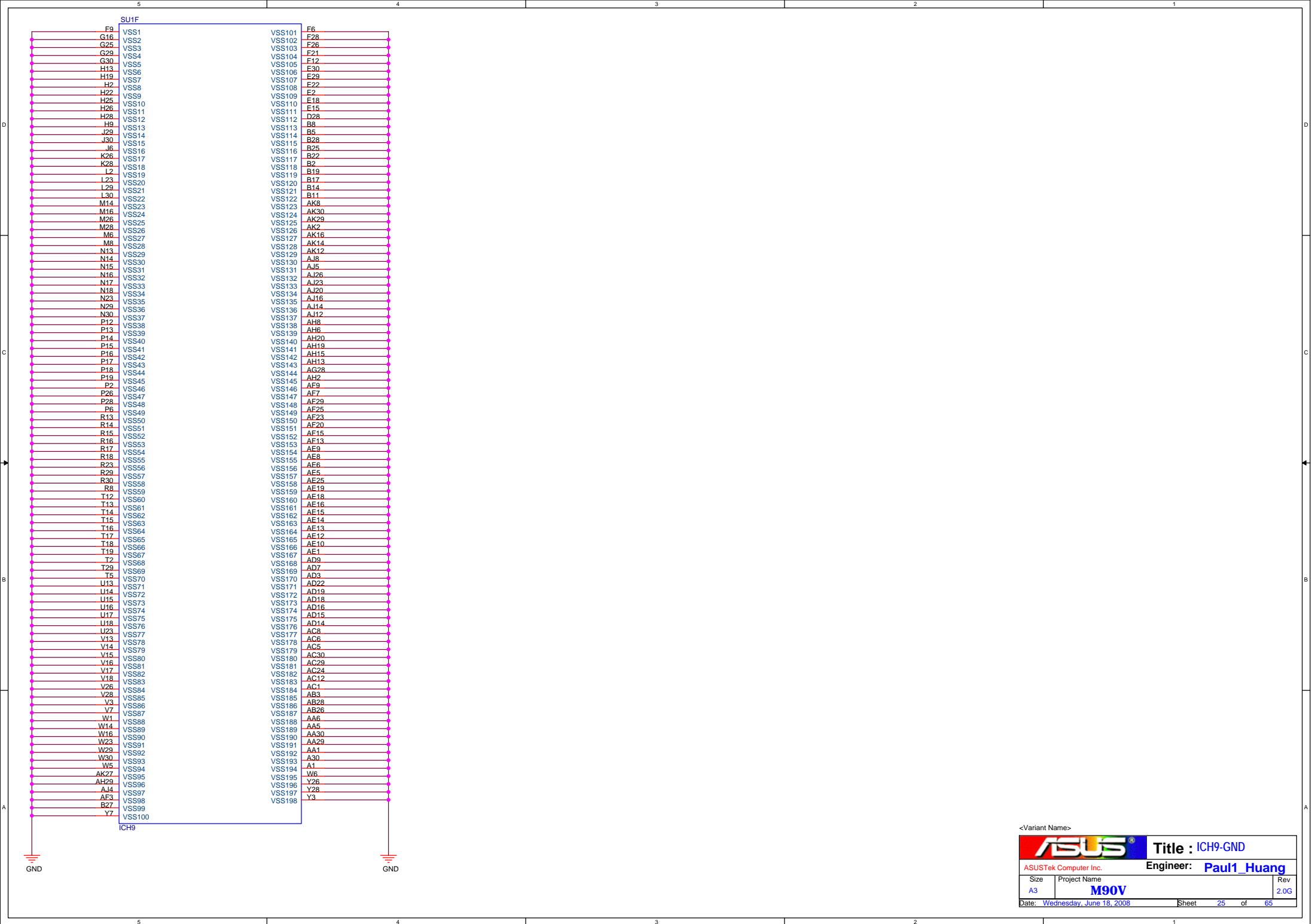
SR75, SR220由15K改爲100K確保準位不會過低

11 = 1 x4, Port 1 (x4)
 10 = Reserved
 01 = Reserved
 00 = 4 x1s, Port 1 (x1), Port 2 (x1), Port 3 (x1) and Port 4 (x1)

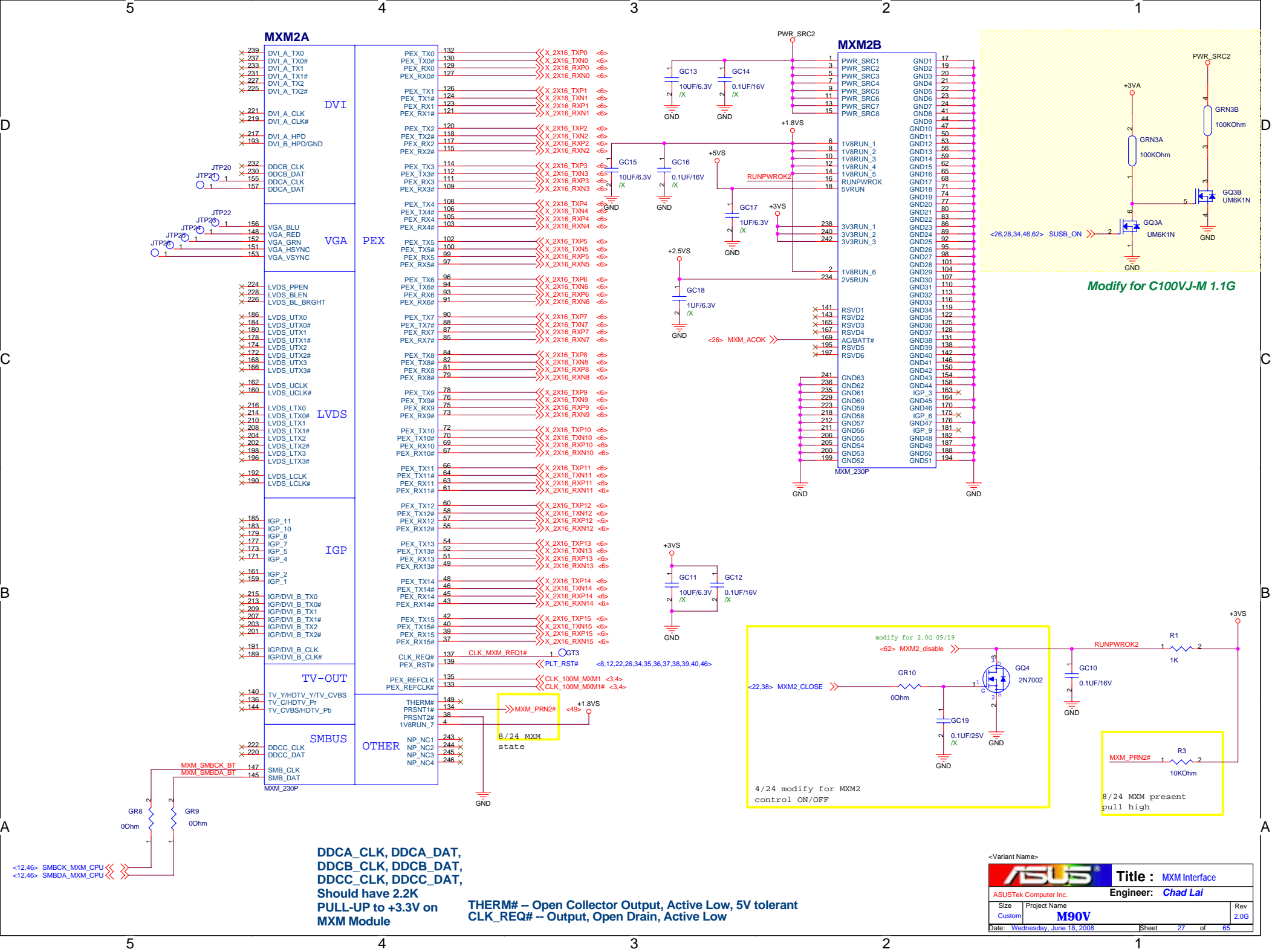


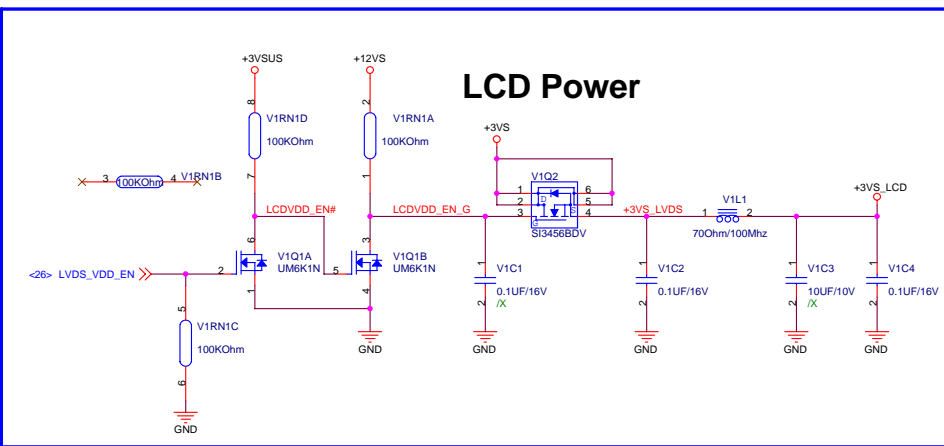








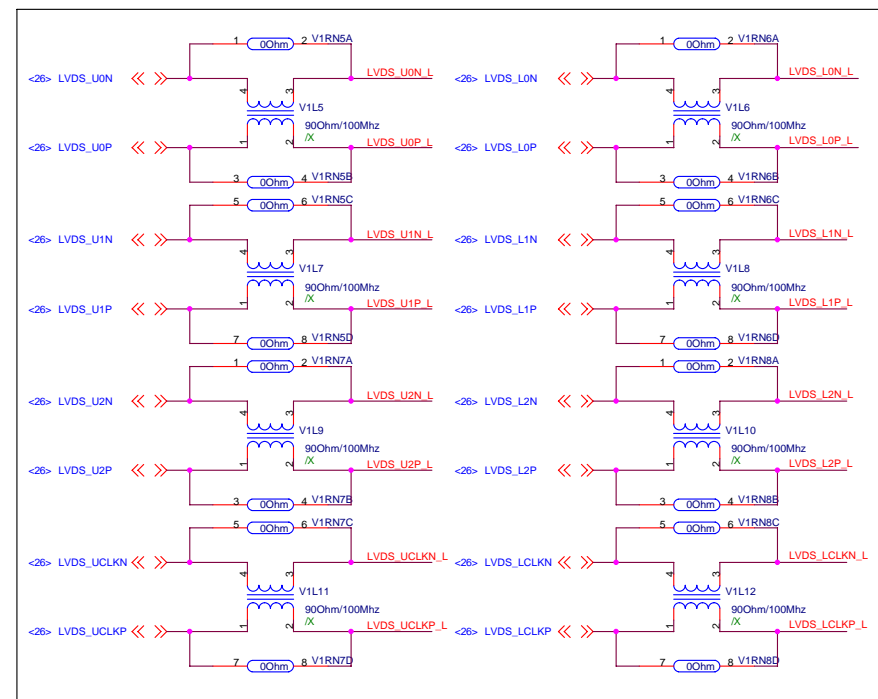
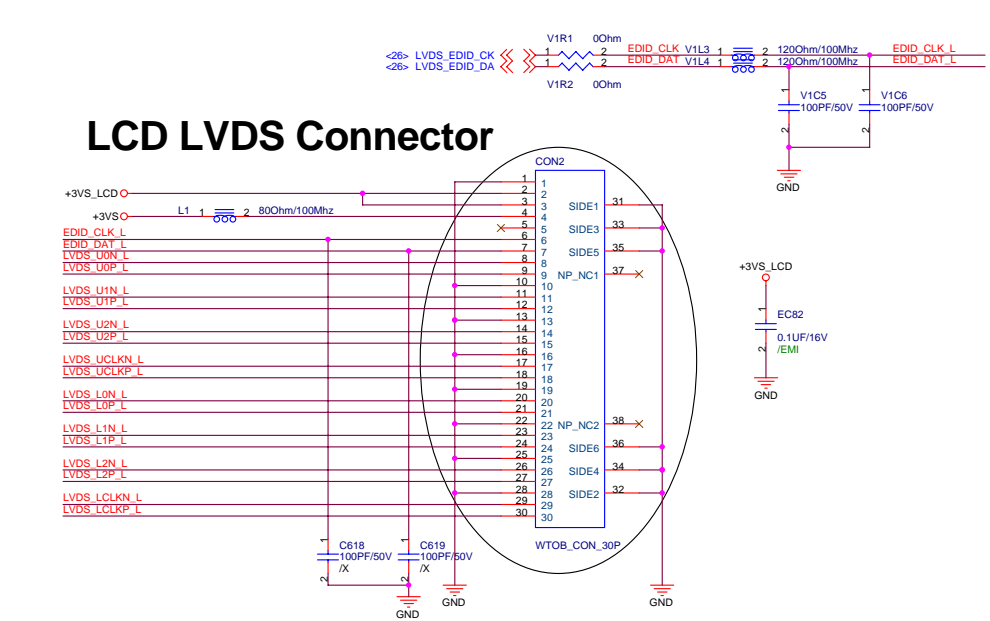
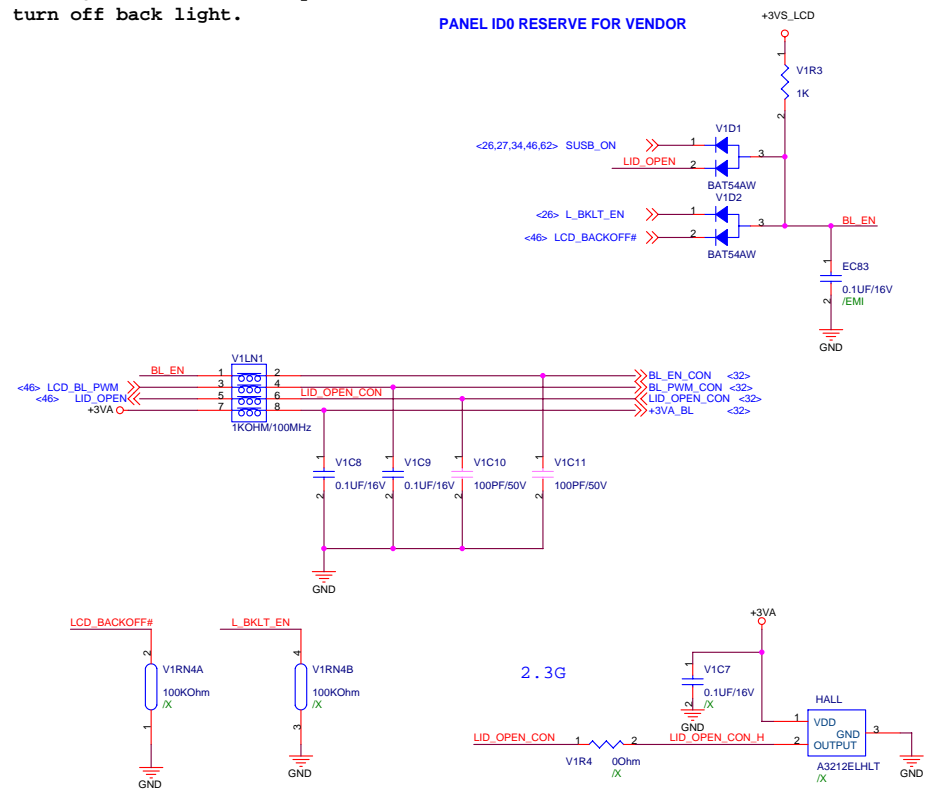


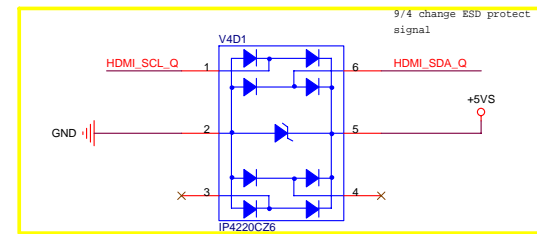


BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.

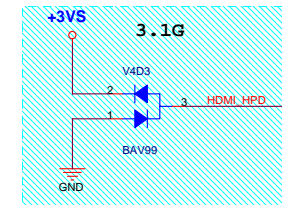
PANEL ID1 = 1 : WSXGA+ 1680x1050
PANEL ID1 = 0 : WXGA 1280x800

PANEL ID0 RESERVE FOR VENDOR

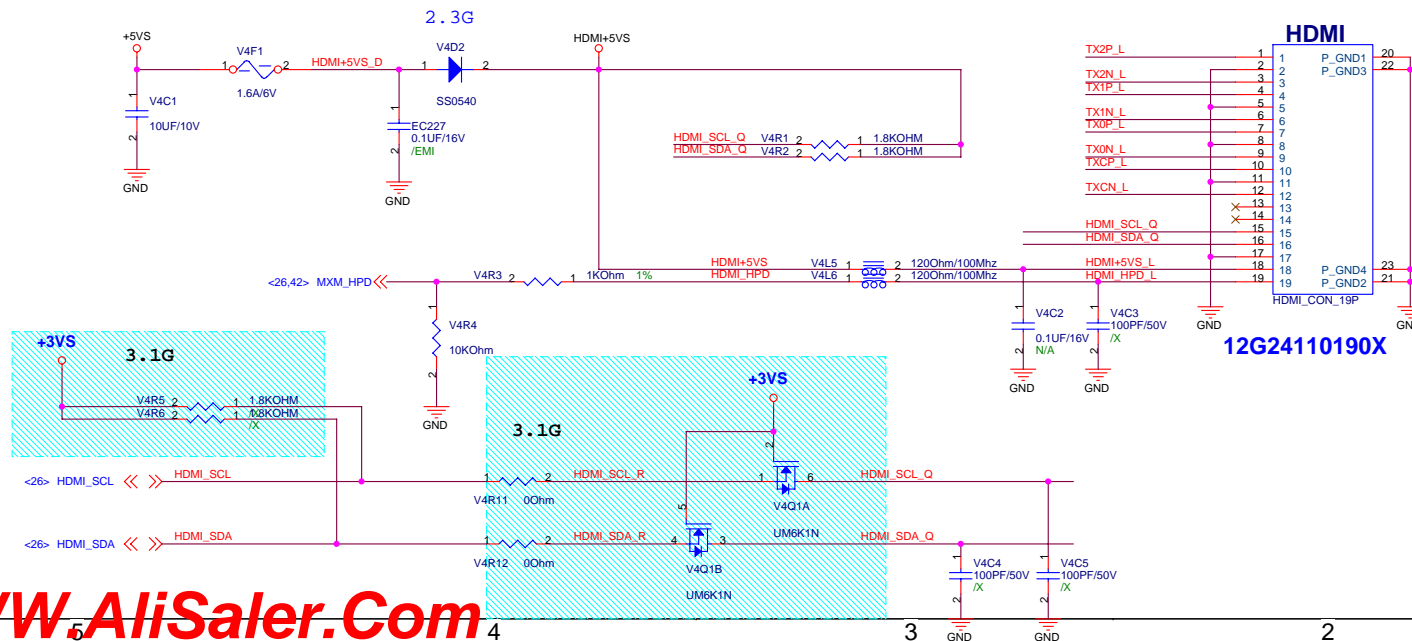




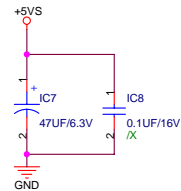
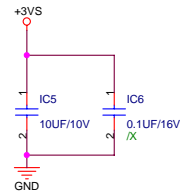
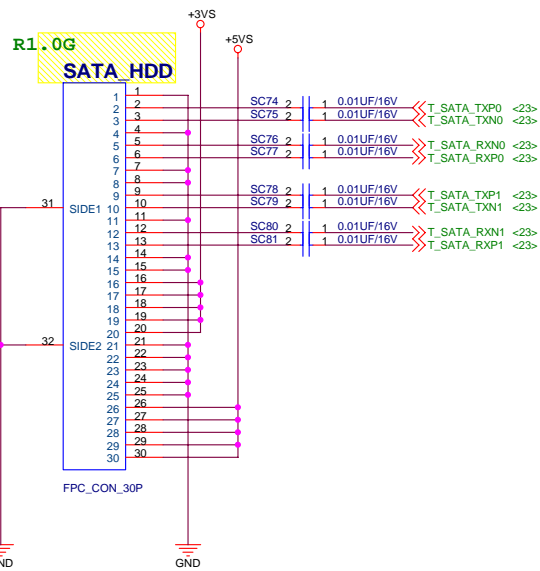
ESD Diode, Place close to Connector



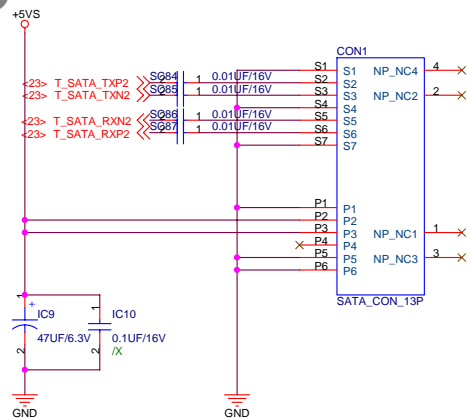
HDMI Connector



ASUS		Title : HDMI Connector	
ASUSTek Computer INC.		Engineer: Chad Lai	
Size	Project Name	M90V	
Custom		Rev 2.0G	
Date: Wednesday, June 18, 2008		Sheet 30	of 65

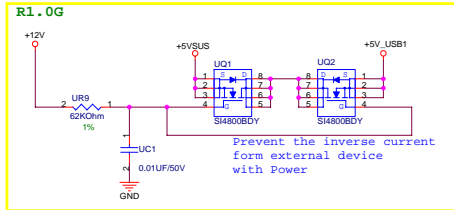


SATA ODD

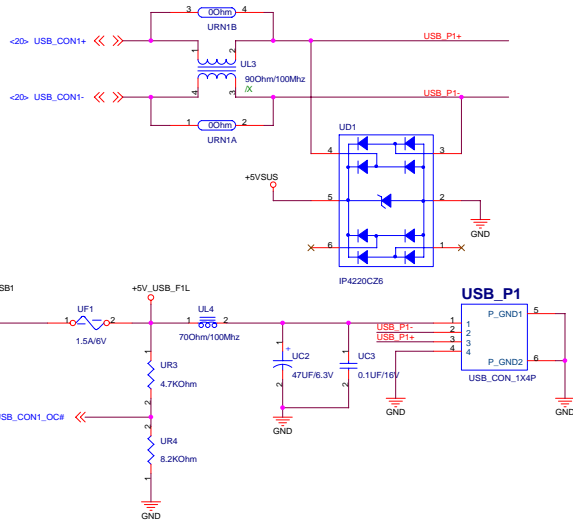


<Variant Name>

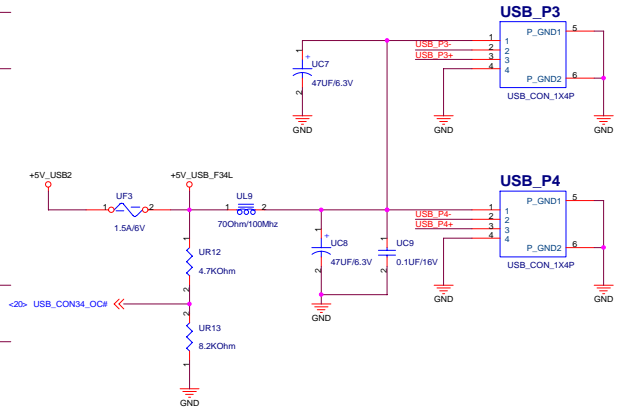
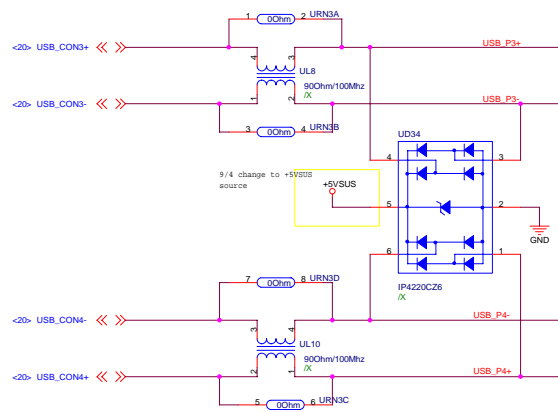
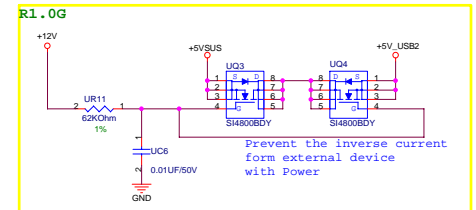
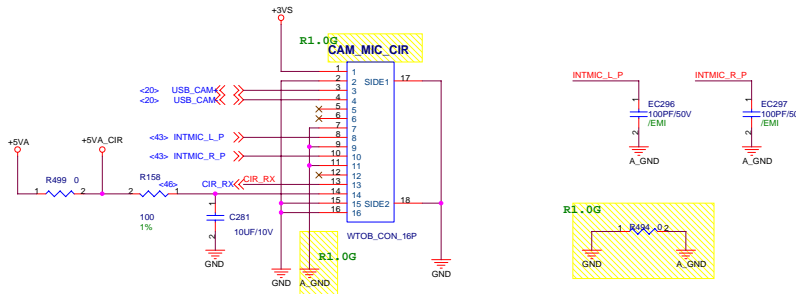
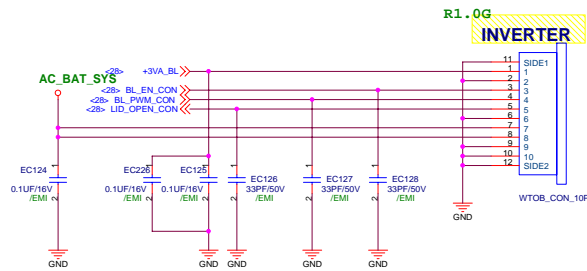
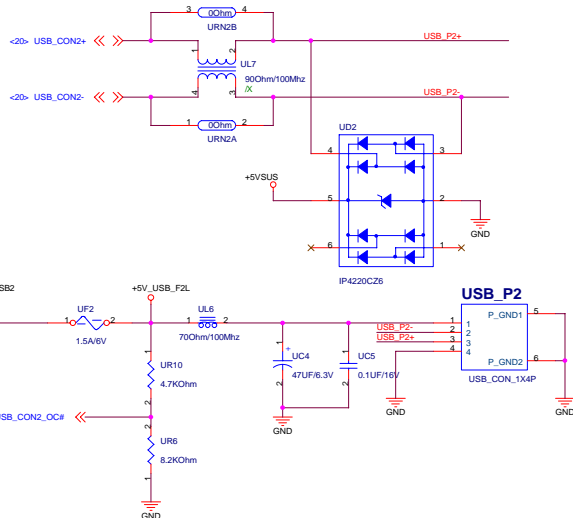
ASUS		Title : SATA-HDD & ODD	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	M90V	2.0G	
Date: Wednesday, June 18, 2008	Sheet	31	of 65



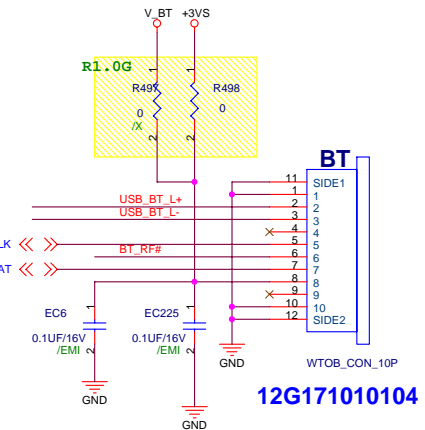
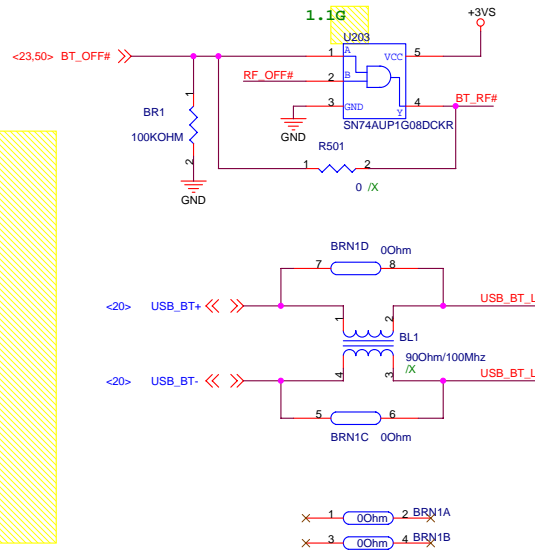
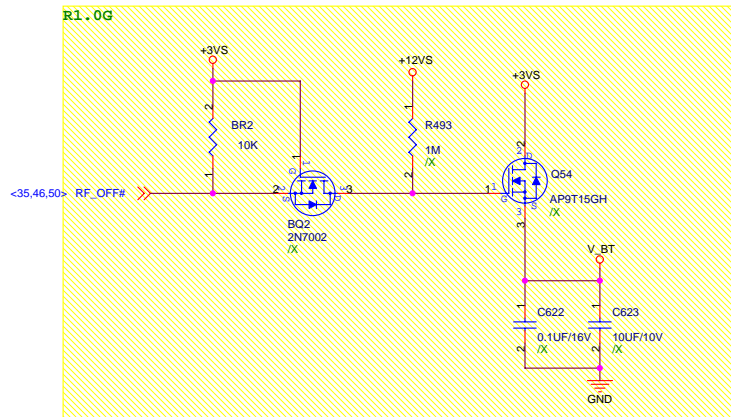
All close to USB connectors



All close to USB connectors

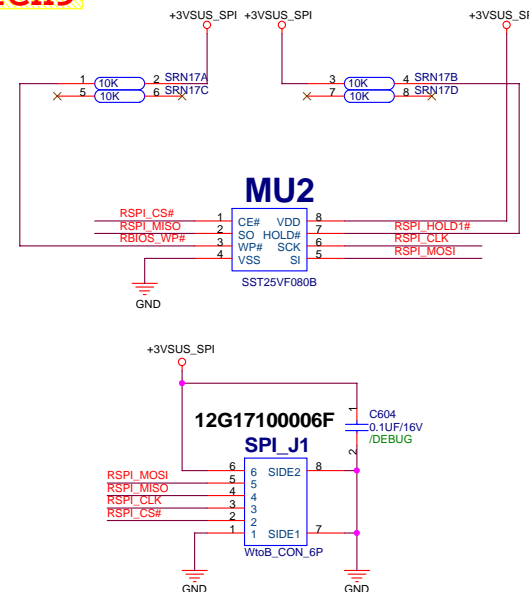
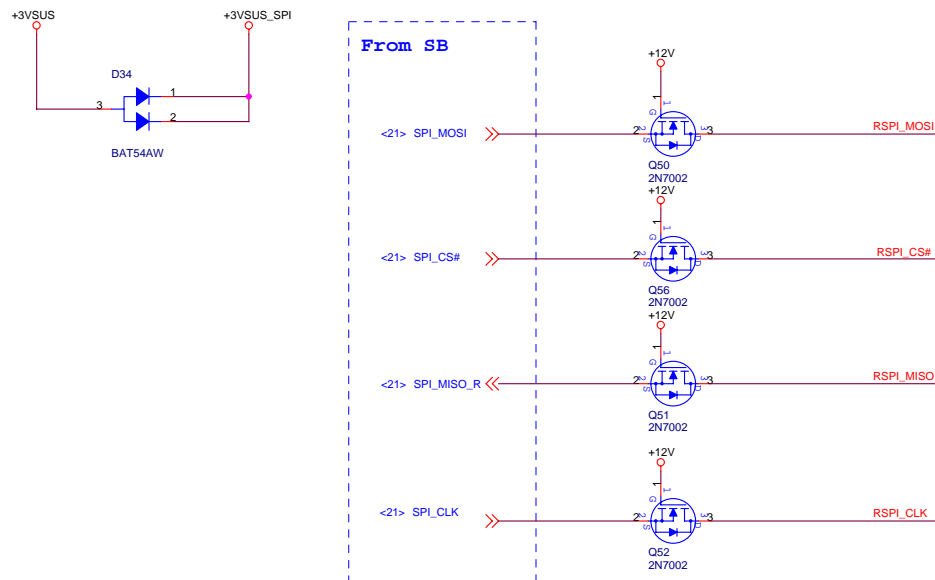


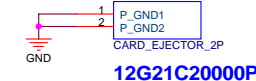
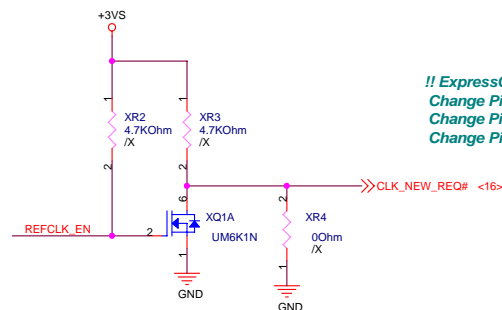
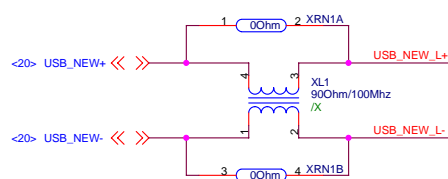
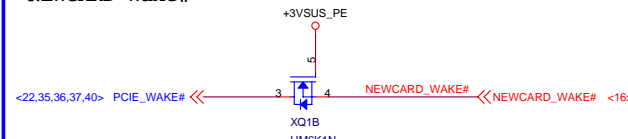
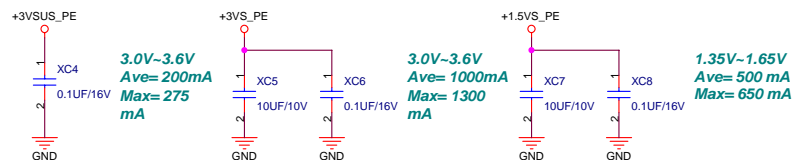
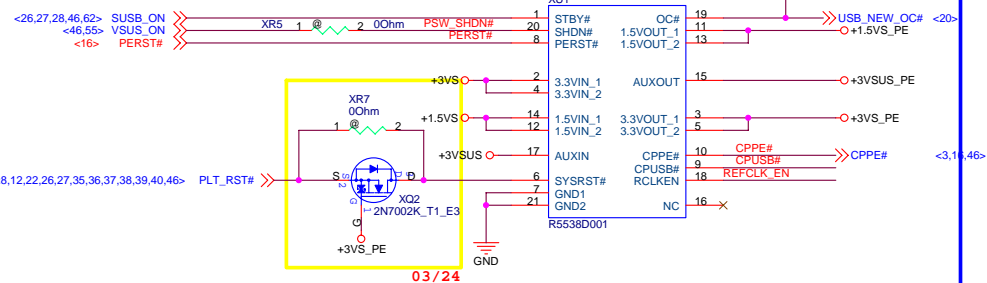
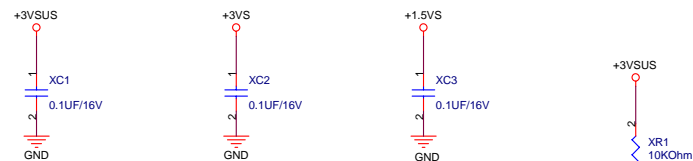
Bluetooth Connector



BT_OFF# : (connect to GPO, push-pull, default High)
0 => BT Disabled
1 => BT Enabled

SPI Close To ICH9





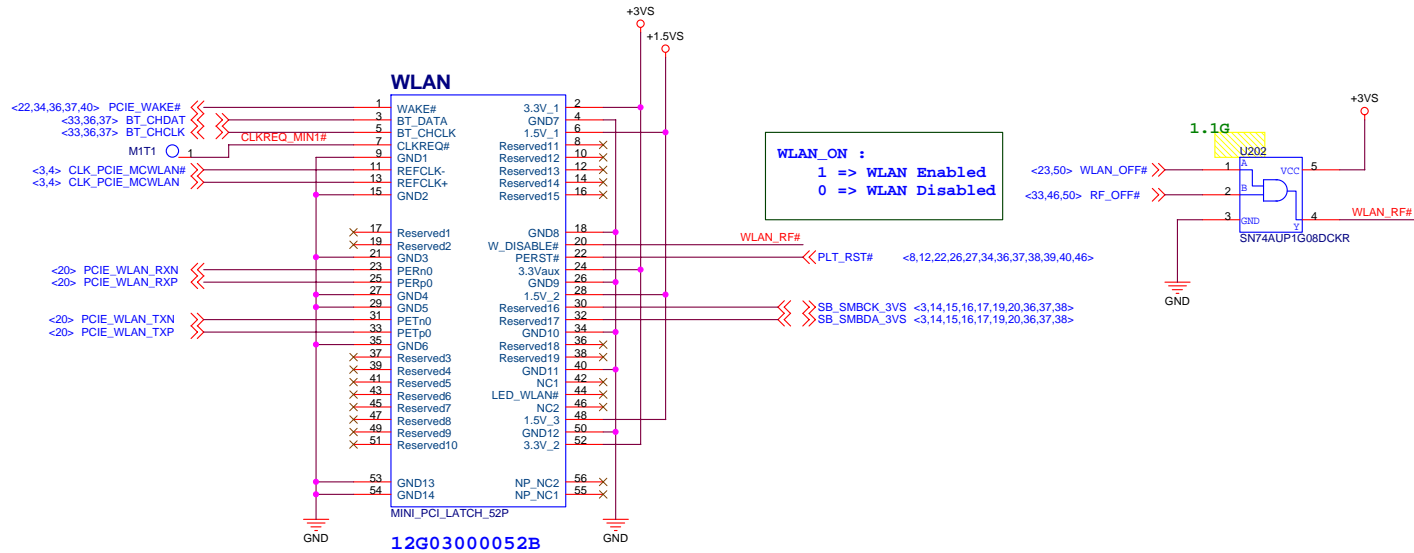
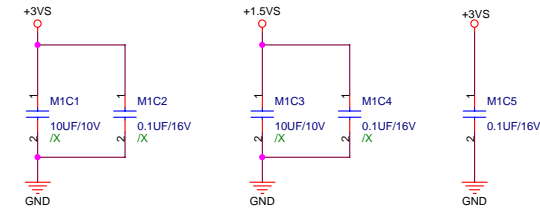
!! ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

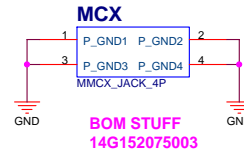
+3.003V~+3.597V
Max= 250 mA



<Variant Name>

ASUS		Title : MINI CARD	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	M90V	2.0G	
Date: Wednesday, June 18, 2008		Sheet	35 of 65

+3.003V~+3.597V
Max= 250 mA



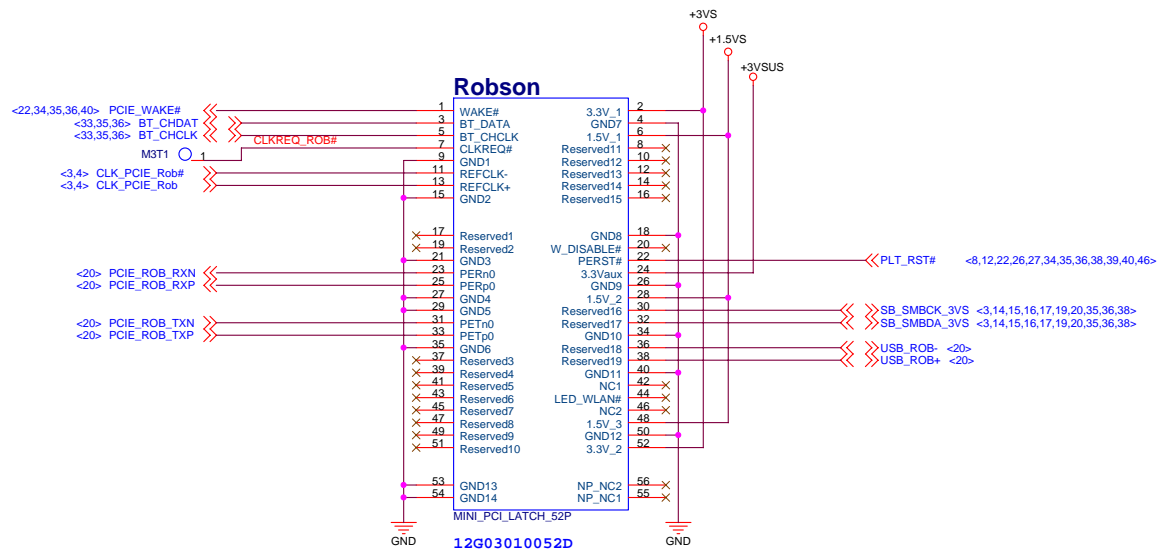
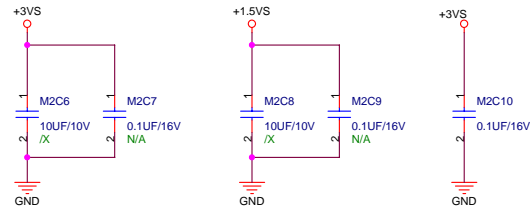
Sheet 36 of 65

Decouple Cap. (Near C_MINICARD1)

+3.003V~+3.597V
Max= 750 mA

+1.425V~+1.575V
Max= 375 mA

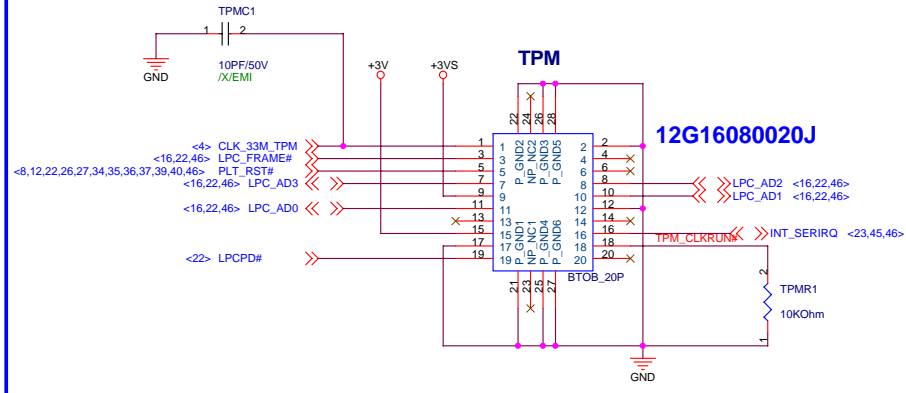
+3.003V~+3.597V
Max= 250 mA



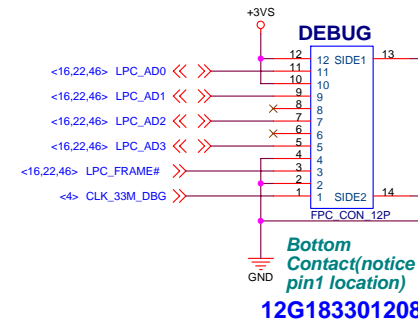
<Variant Name>

ASUS		Title : MINI CARD	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	M90V	2.0G	
Date: Wednesday, June 18, 2008	Sheet 37 of 65		

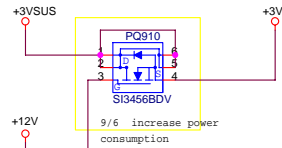
TPM Connector



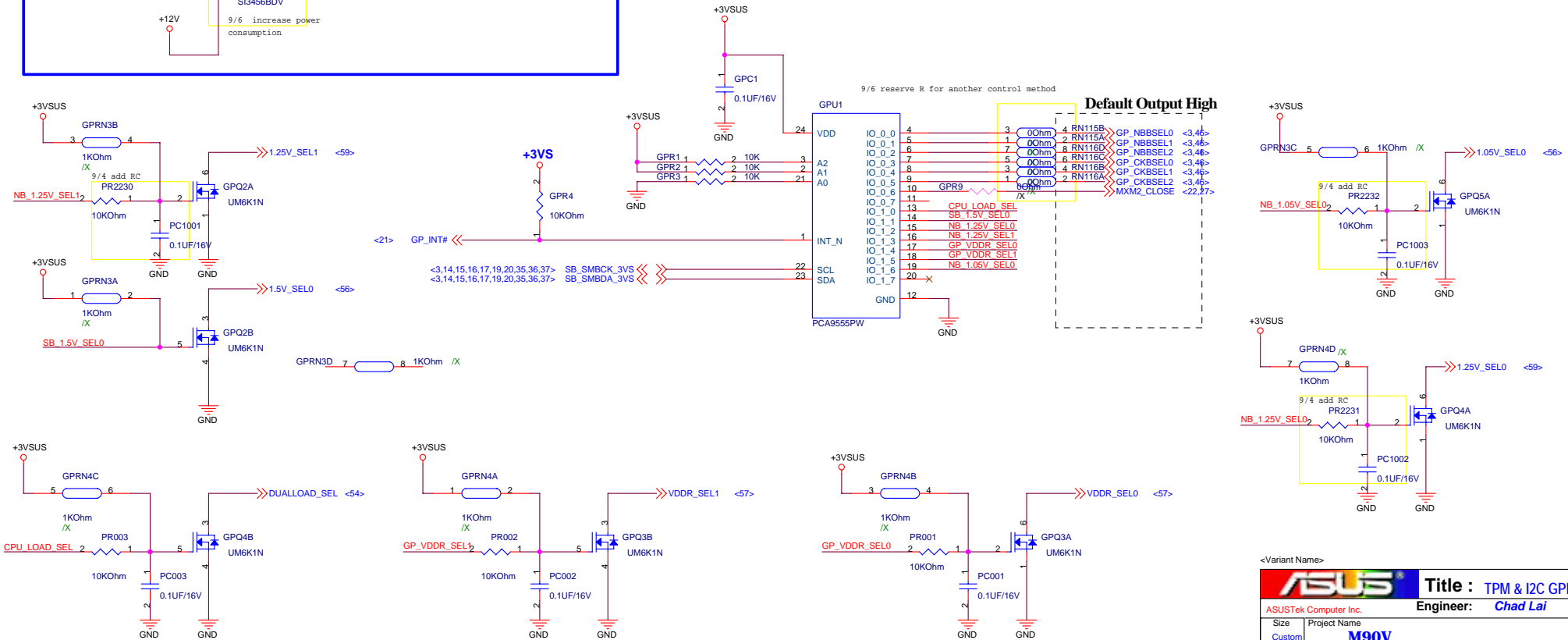
Debug Connector



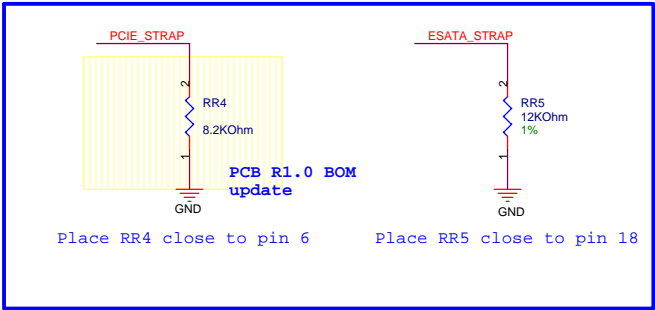
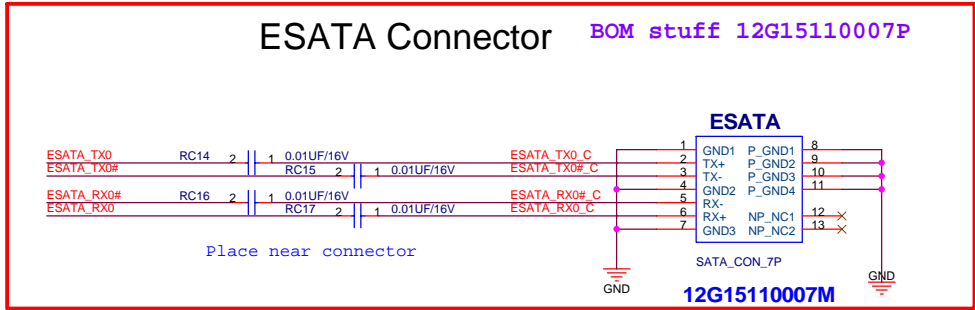
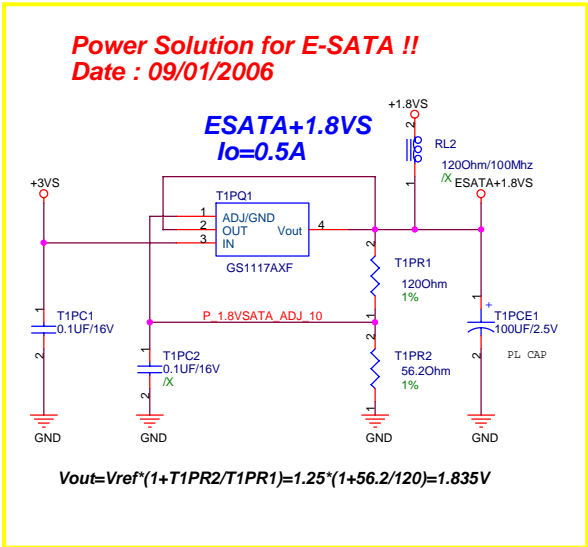
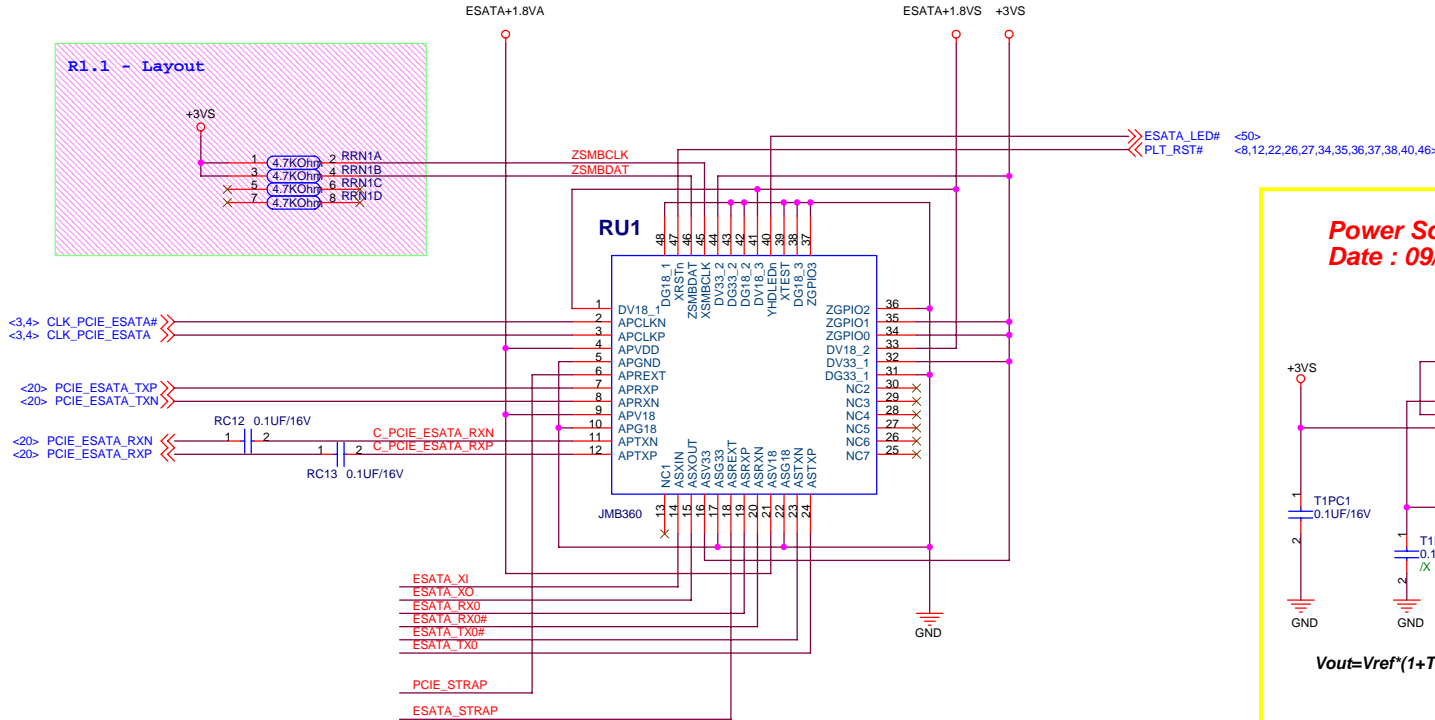
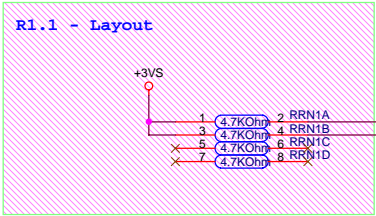
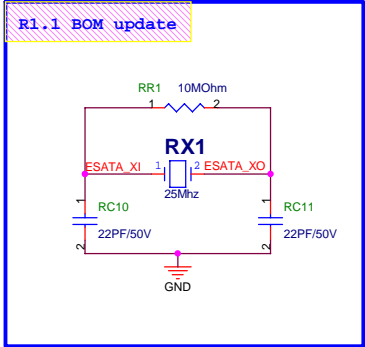
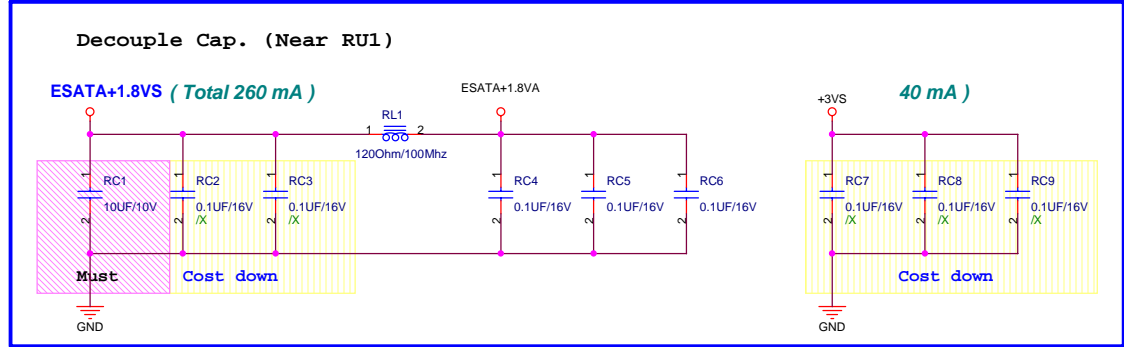
FOR +3V POWER
TPM
PWR_LED

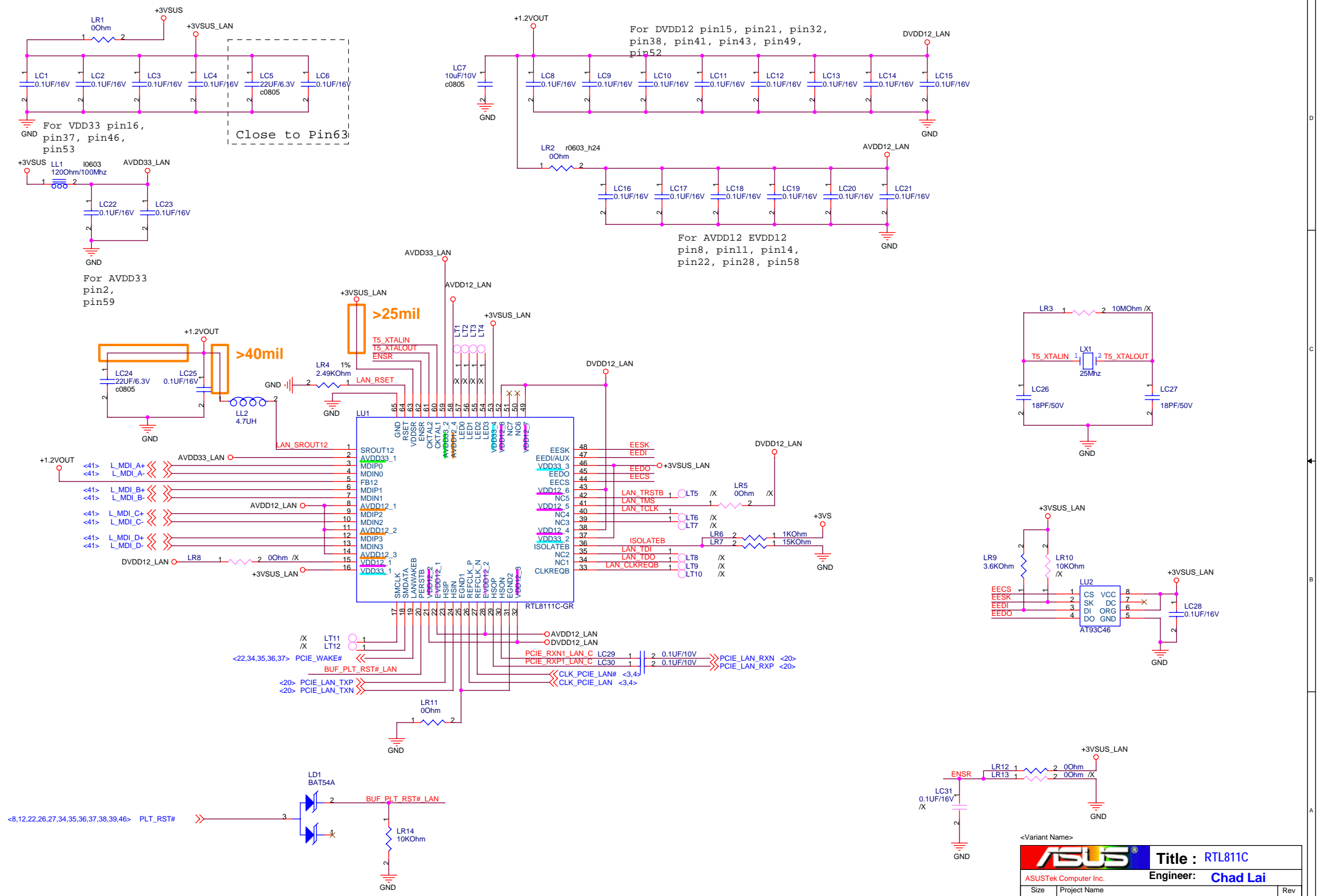


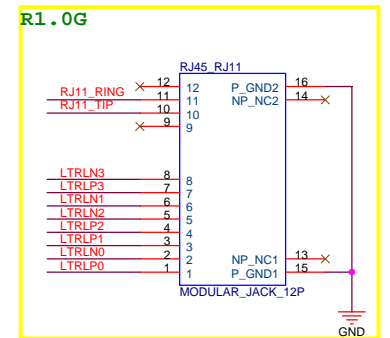
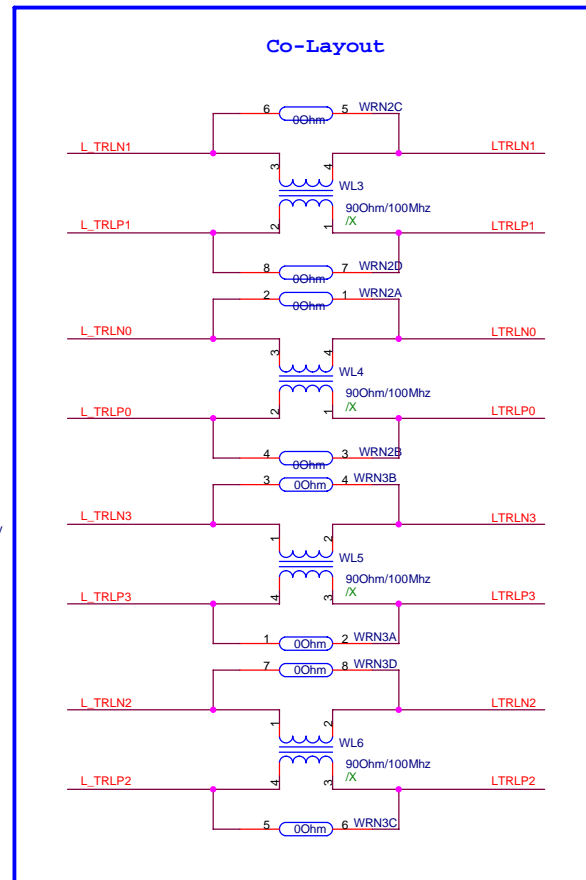
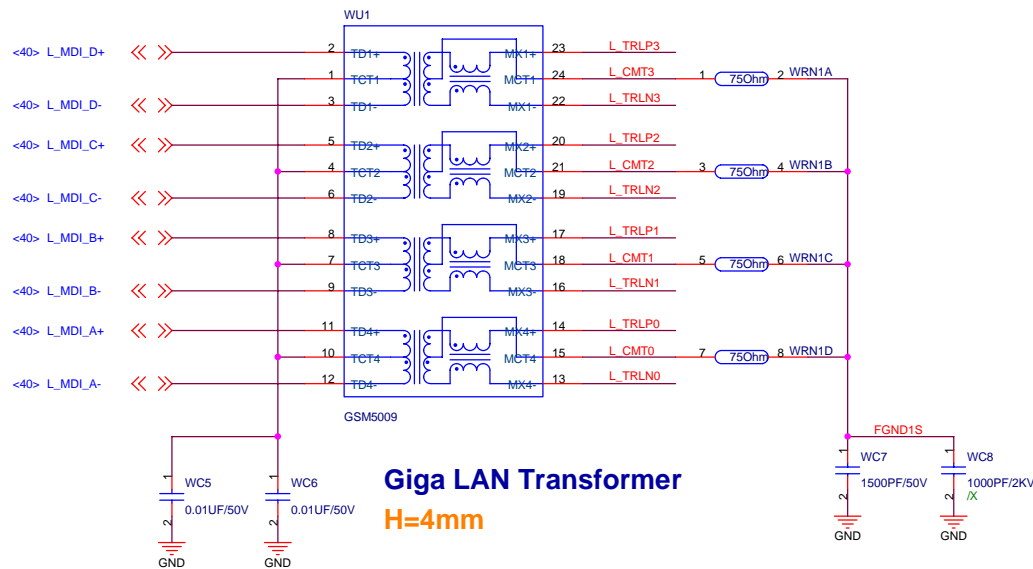
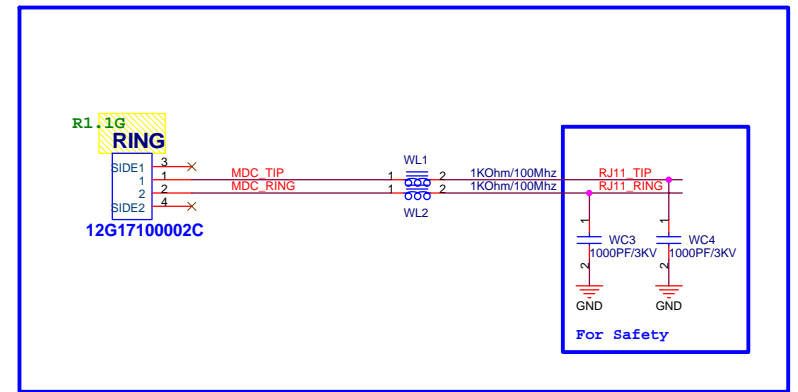
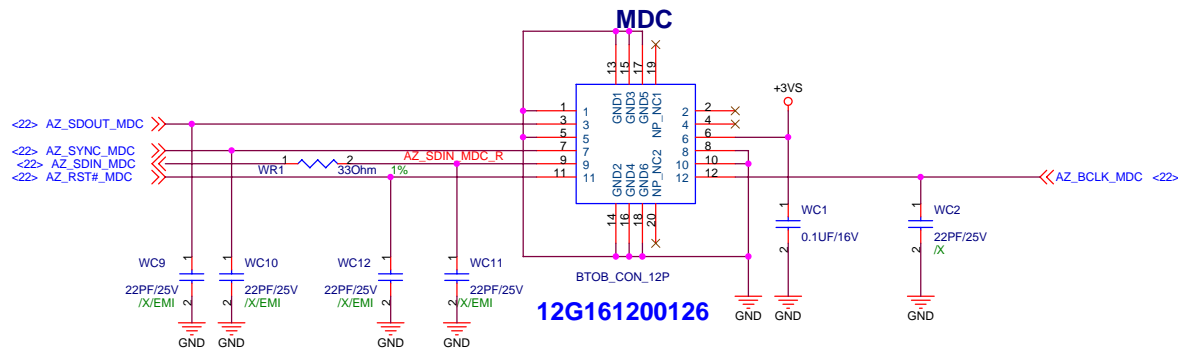
I2C GPIO Controller

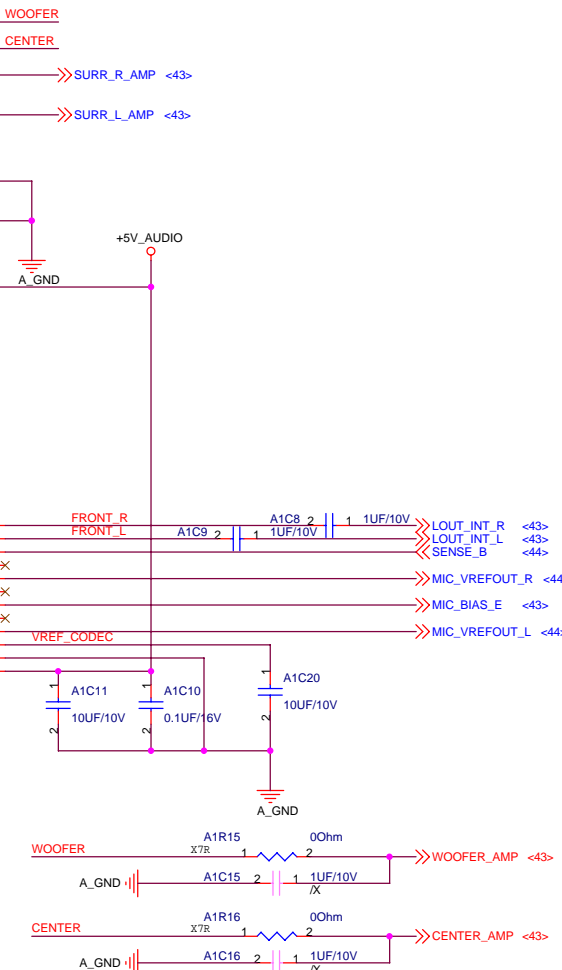
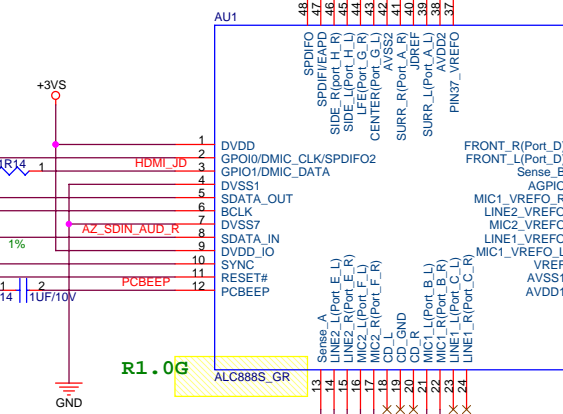
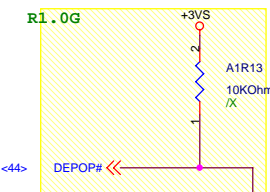
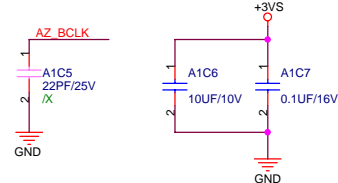
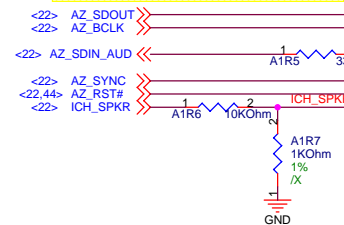
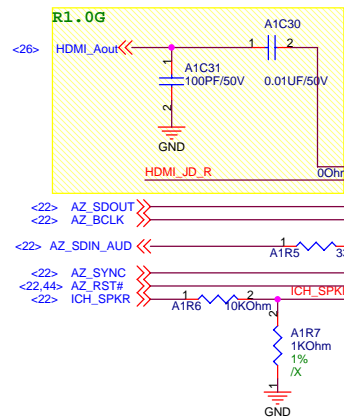
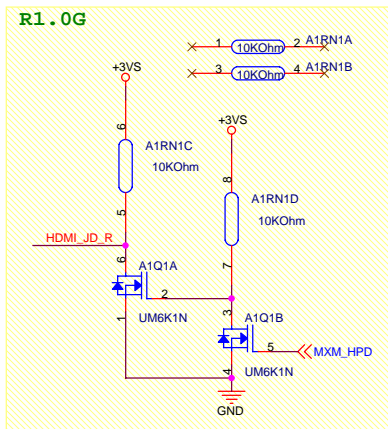
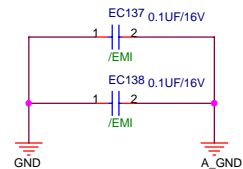
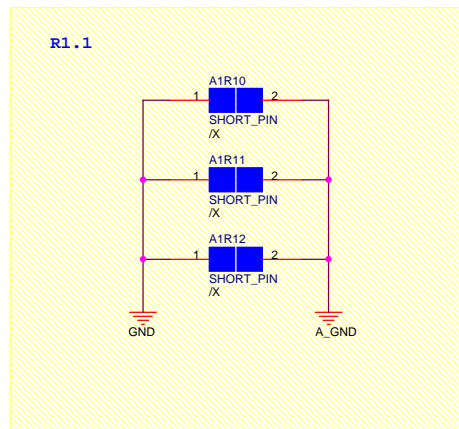
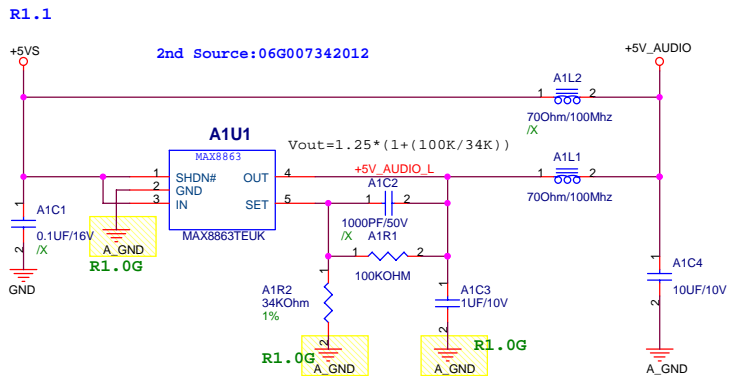


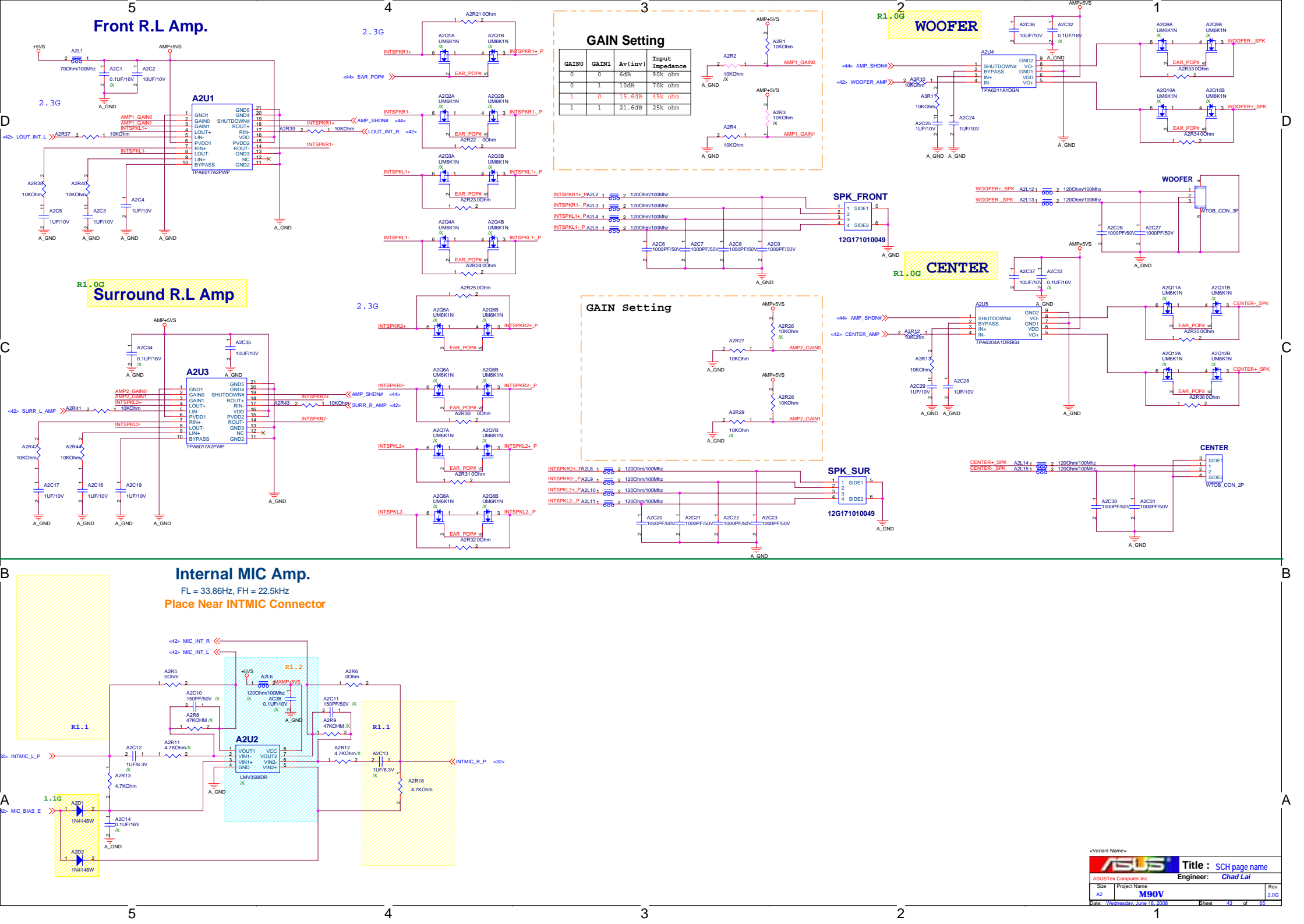
ASUS		Title : TPM & I2C GPIO Controller	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	M90V	2.0G	
Date: Wednesday, June 18, 2008		Sheet	38 of 65

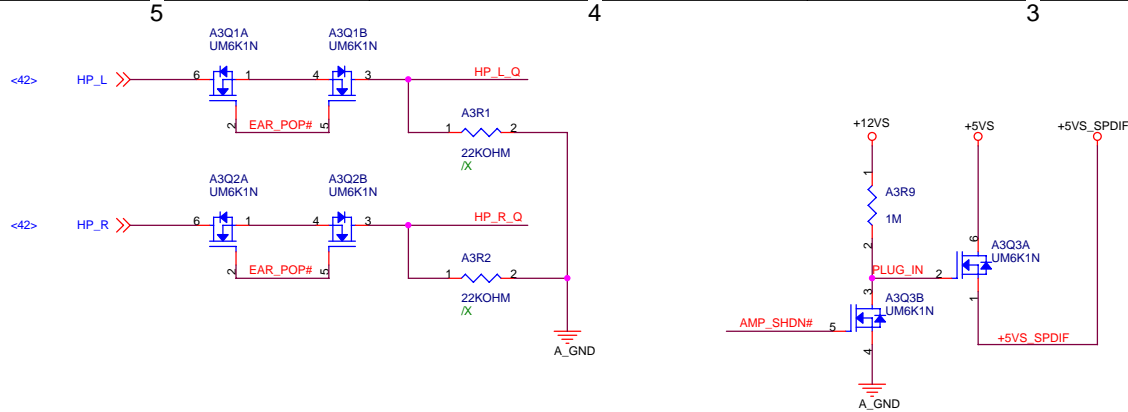




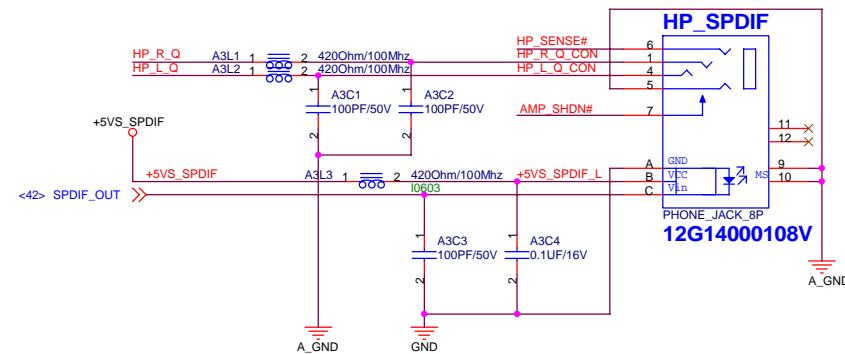






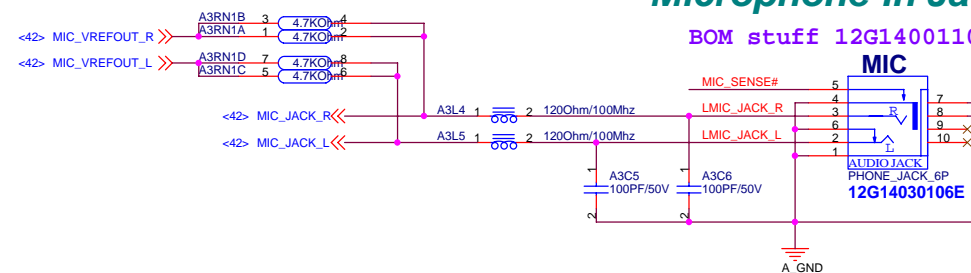


Headphone & S/PDIF Jack

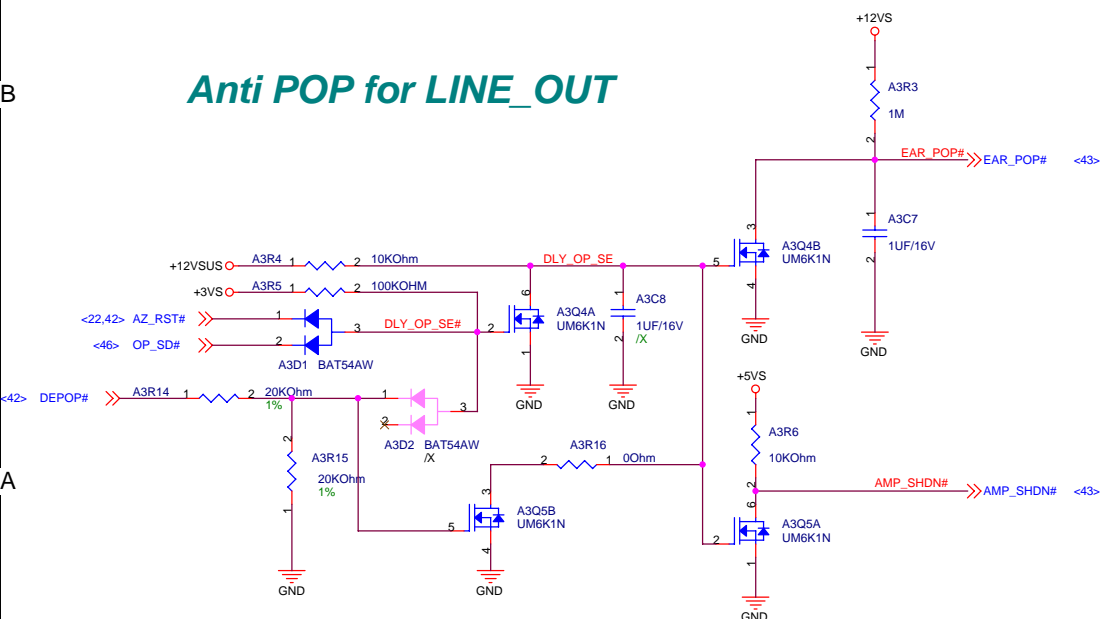


Microphone-In Jack

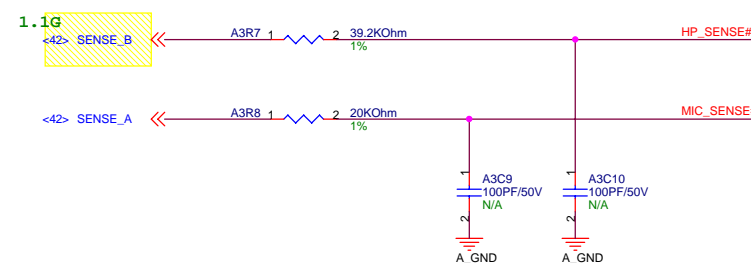
BOM stuff 12G14001106M



Anti POP for LINE_OUT

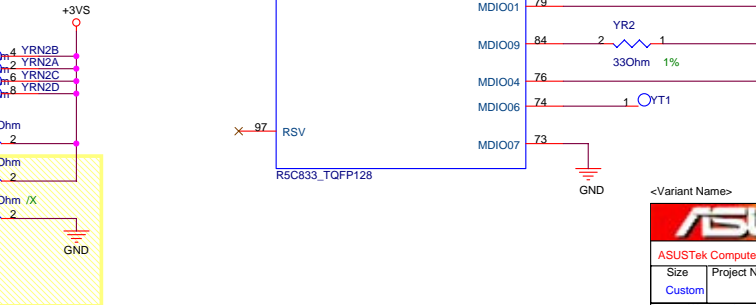
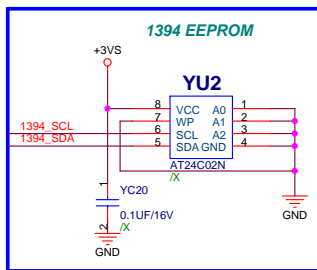
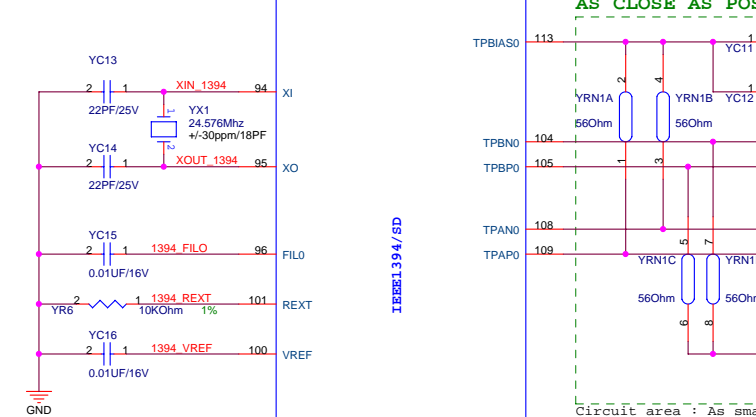
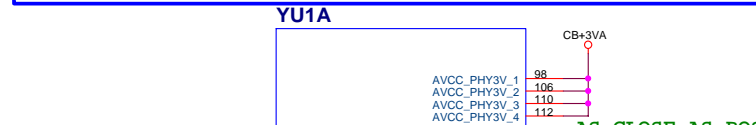


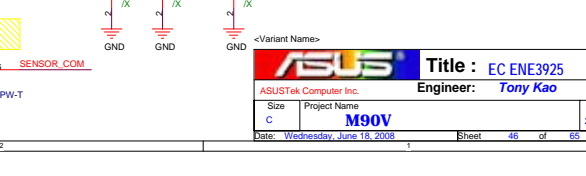
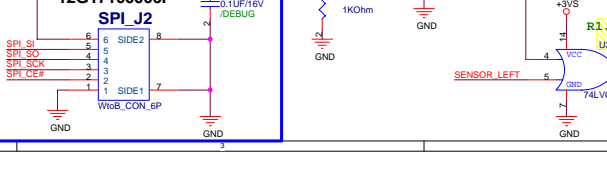
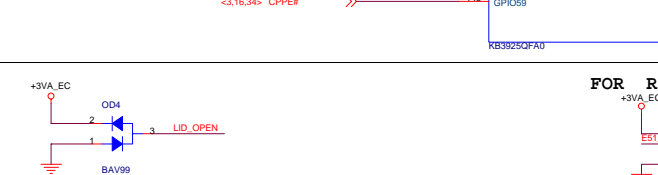
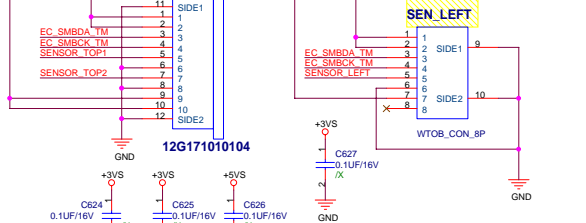
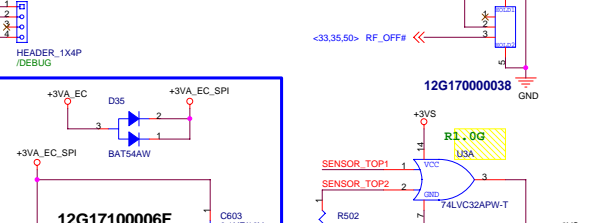
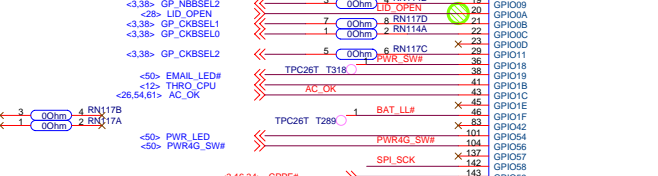
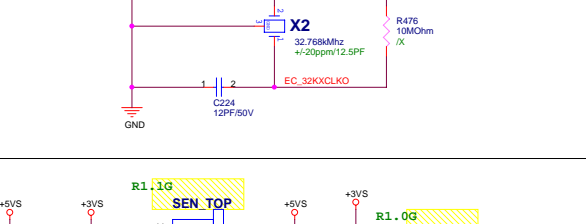
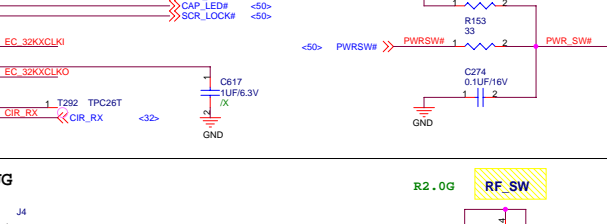
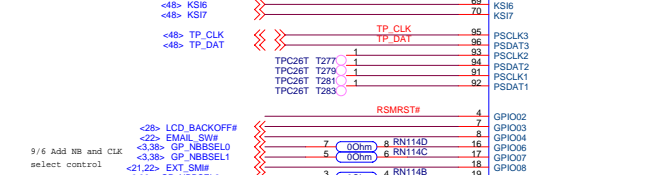
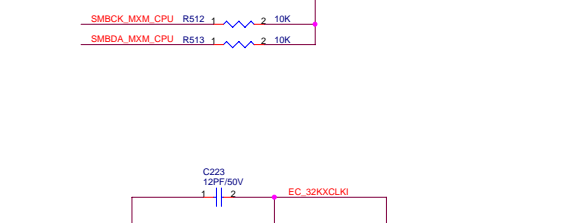
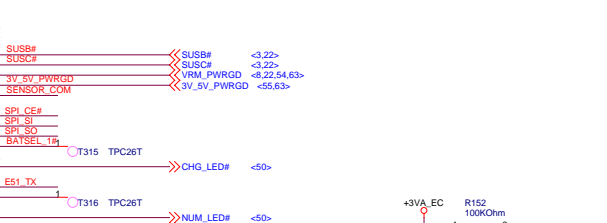
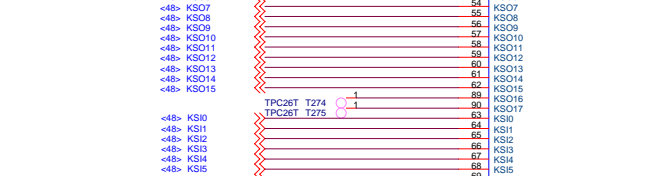
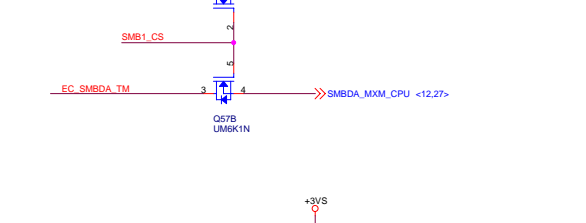
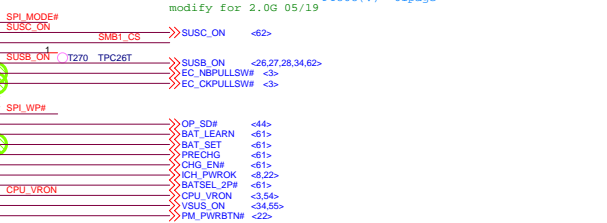
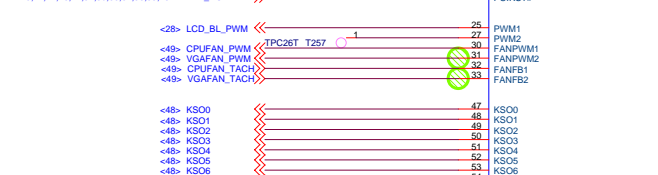
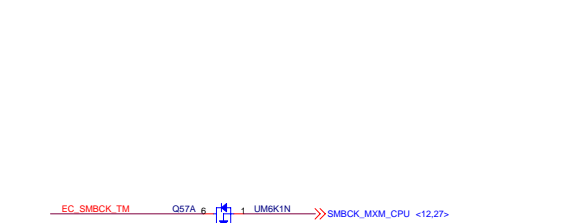
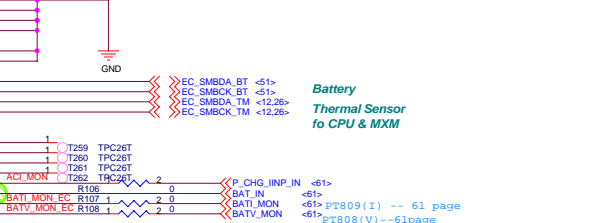
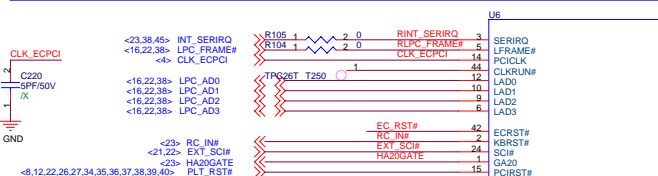
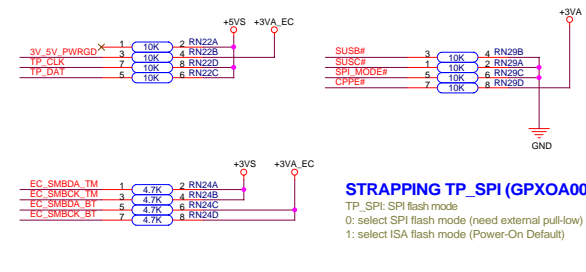
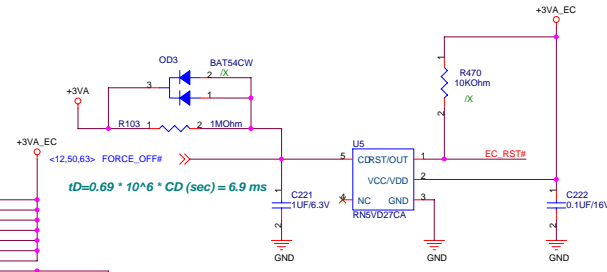
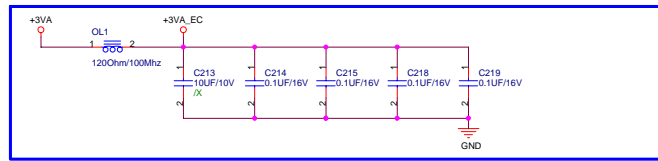
Jack Plug-in Detection



<Variant Name>

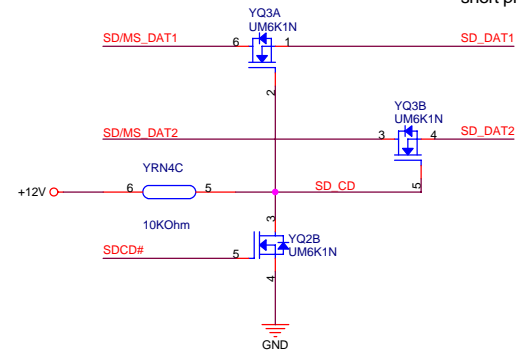
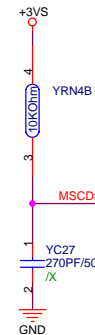
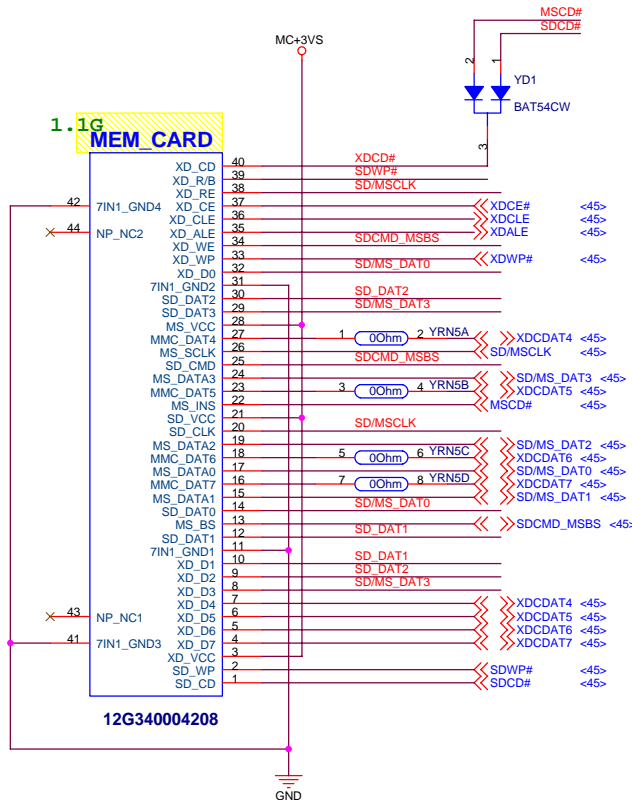
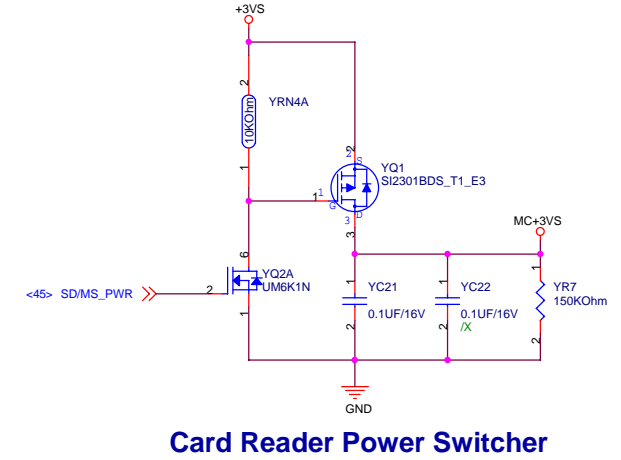
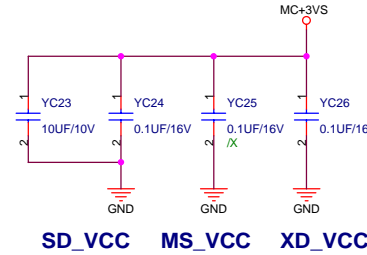
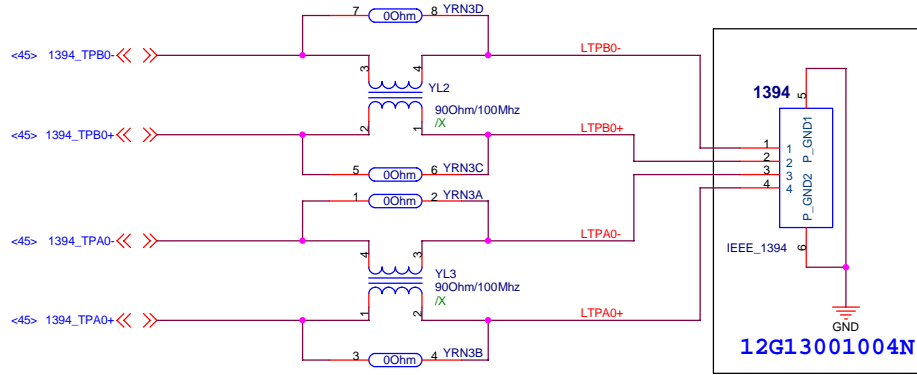
ASUS		Title : SCH page name	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
A3	M90V	2.0G	
Date: Wednesday, June 18, 2008		Sheet 44 of 65	





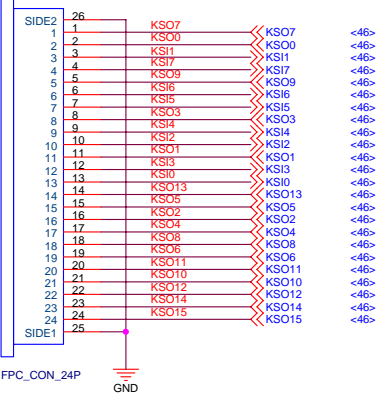
STRAPPING TP_SPI (GPXA00)
TP_SPI: SPI flash mode
0: select SPI flash mode (need external pull-low)
1: select ISA flash mode (Power-On Default)

1394

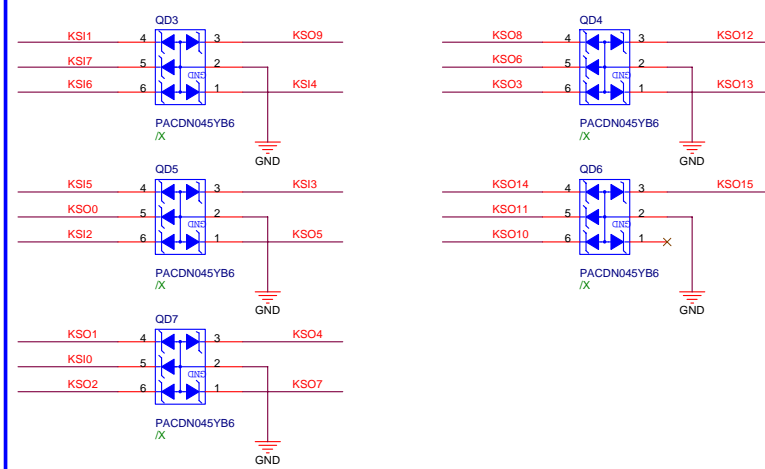


R1.0G KB

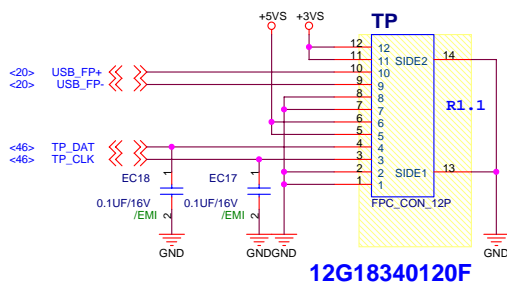
Keyboard Connector



FOR EMI/ESD

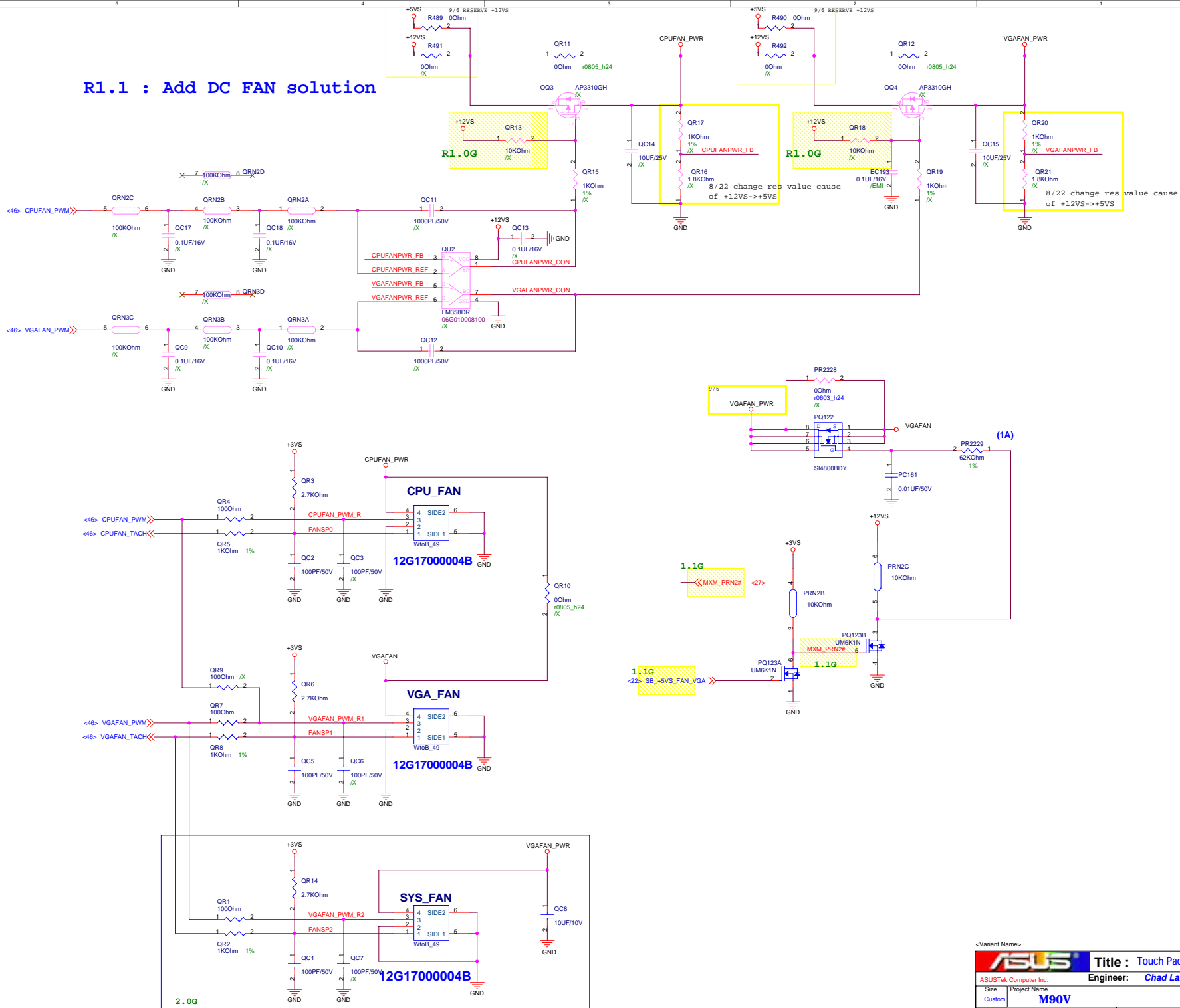


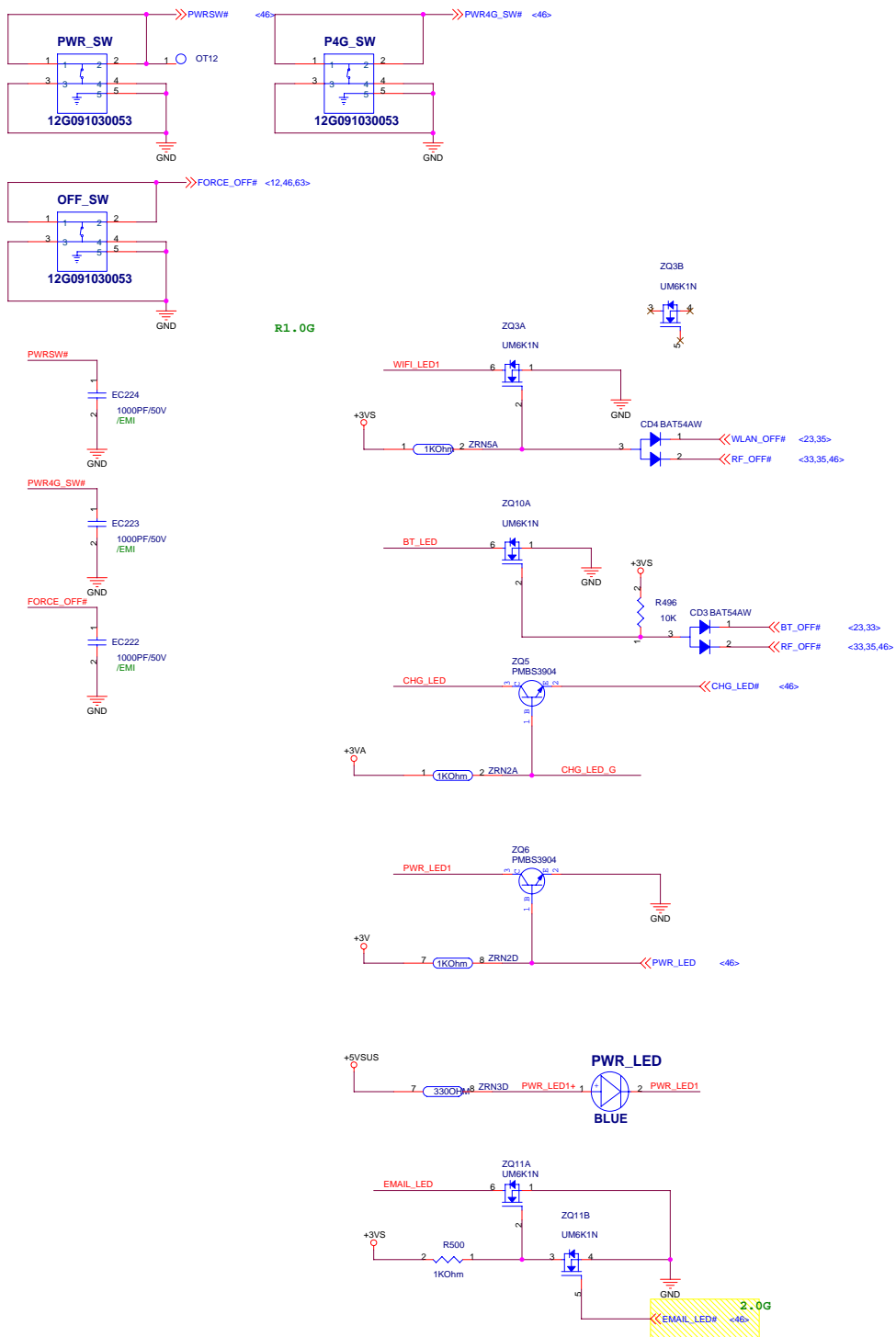
Fingerprint & TouchPad Connector



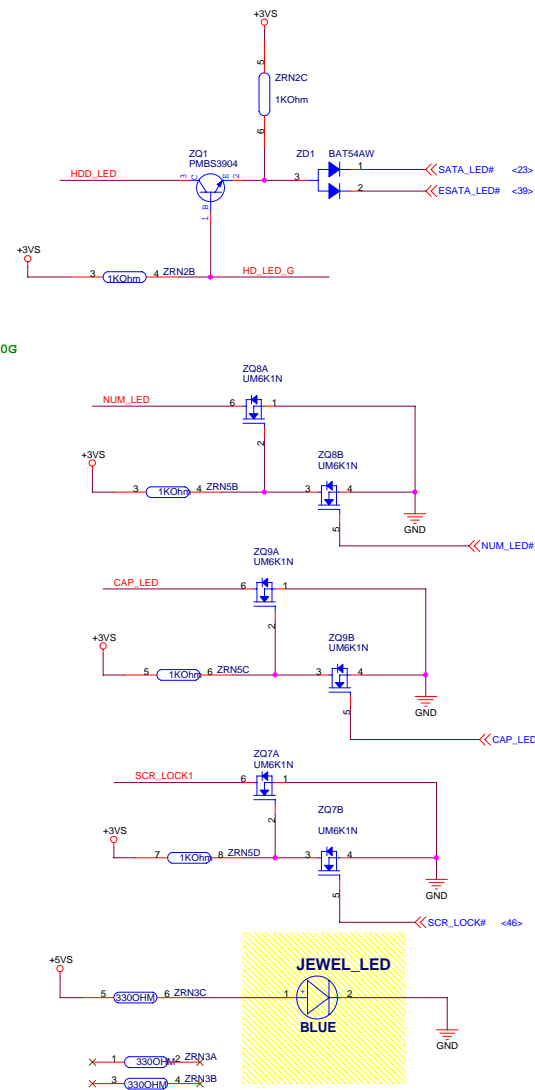
<Variant Name>

R1.1 : Add DC FAN solution

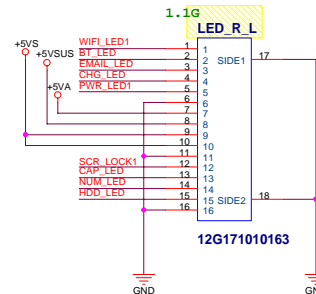




R1.0G



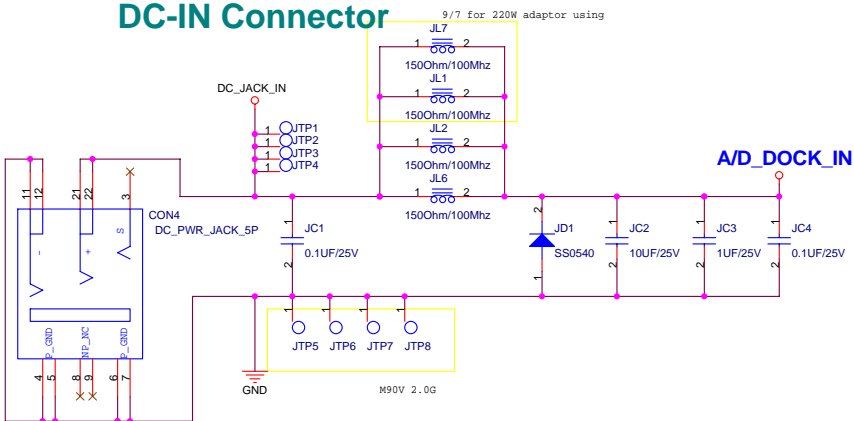
1.1G



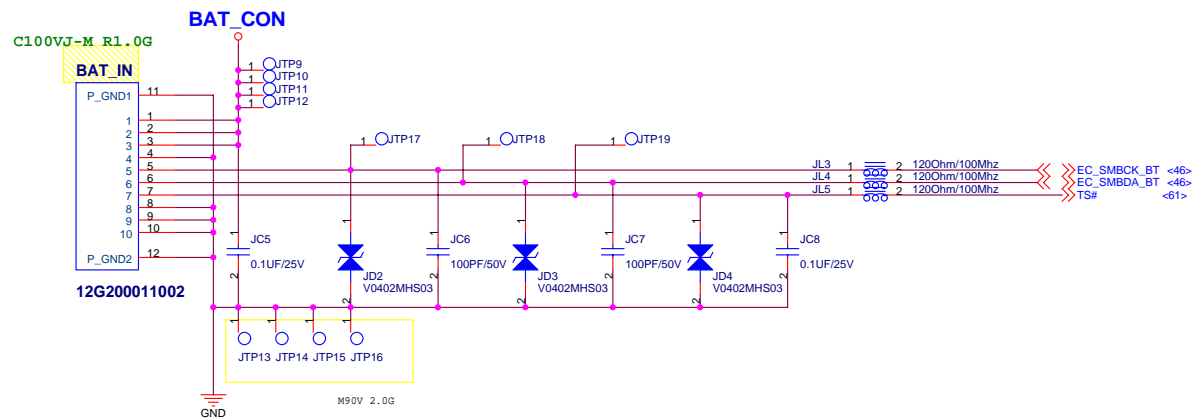
<Variant Name>

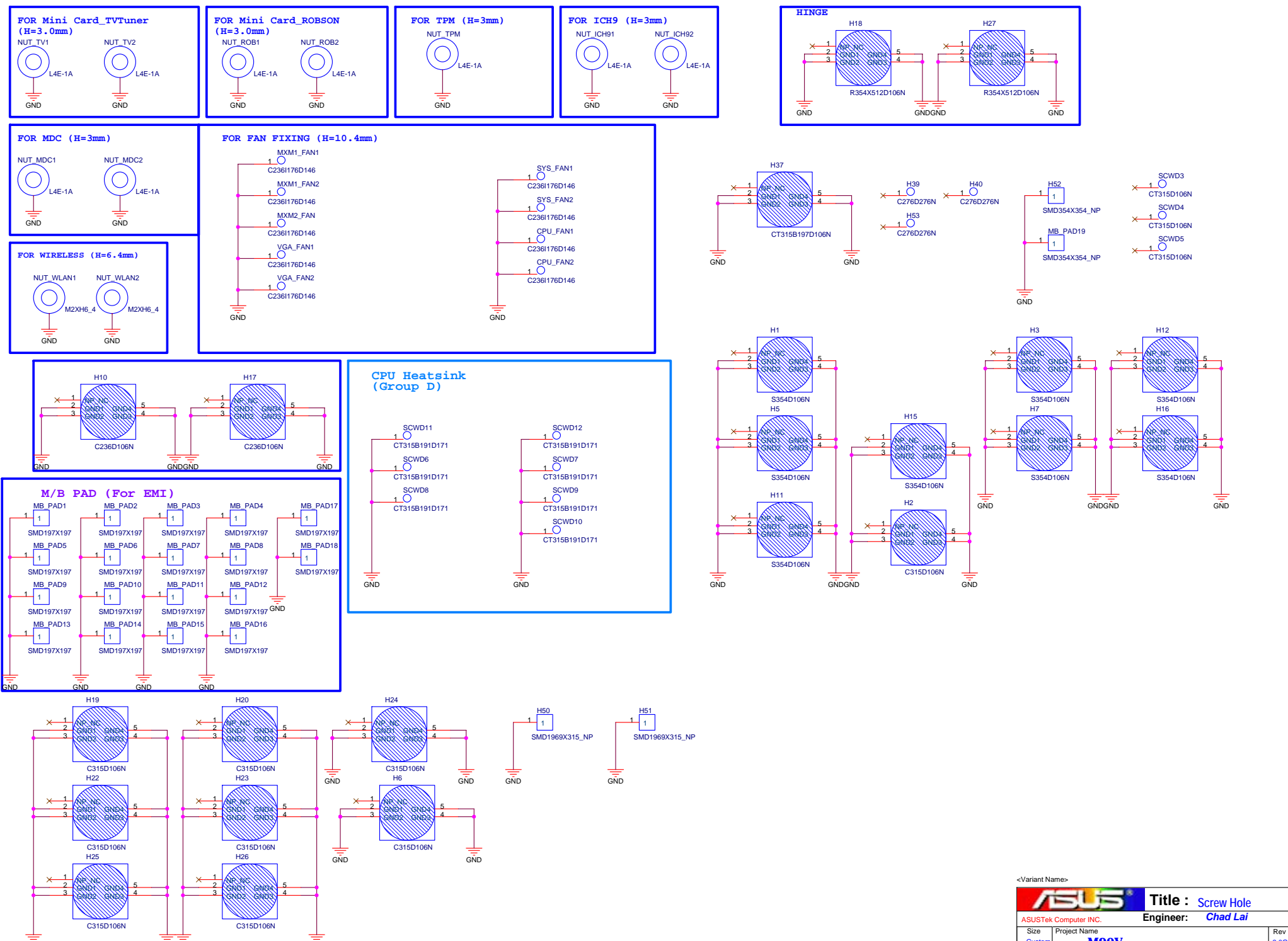
ASUS		Title : LED & SW	
ASUSTek Computer Inc.		Engineer: Chad Lai	
Size	Project Name	Rev	
Custom	M90V	2.0G	
Date: Wednesday, June 18, 2008		Sheet	50 of 65

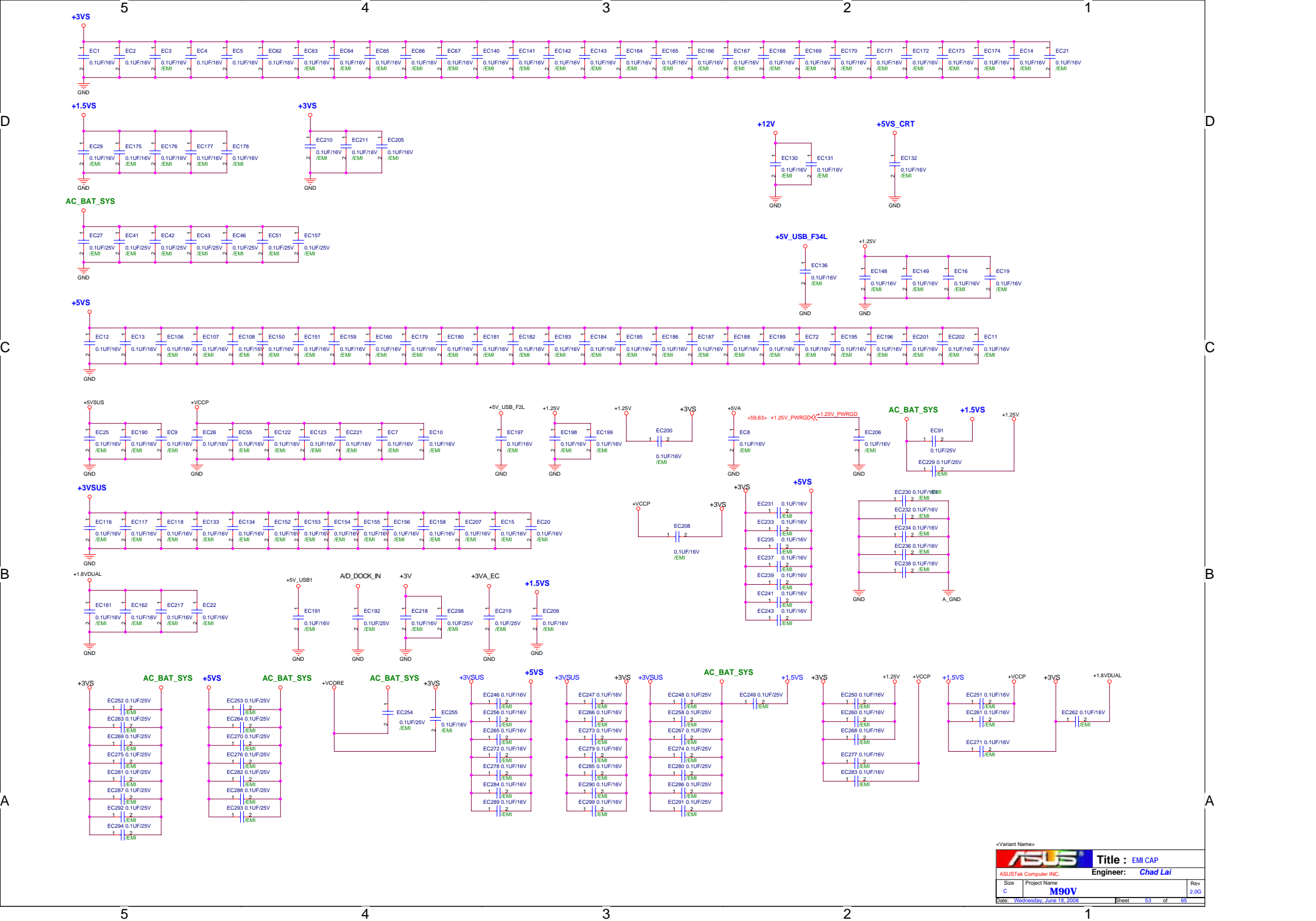
DC-IN Connector

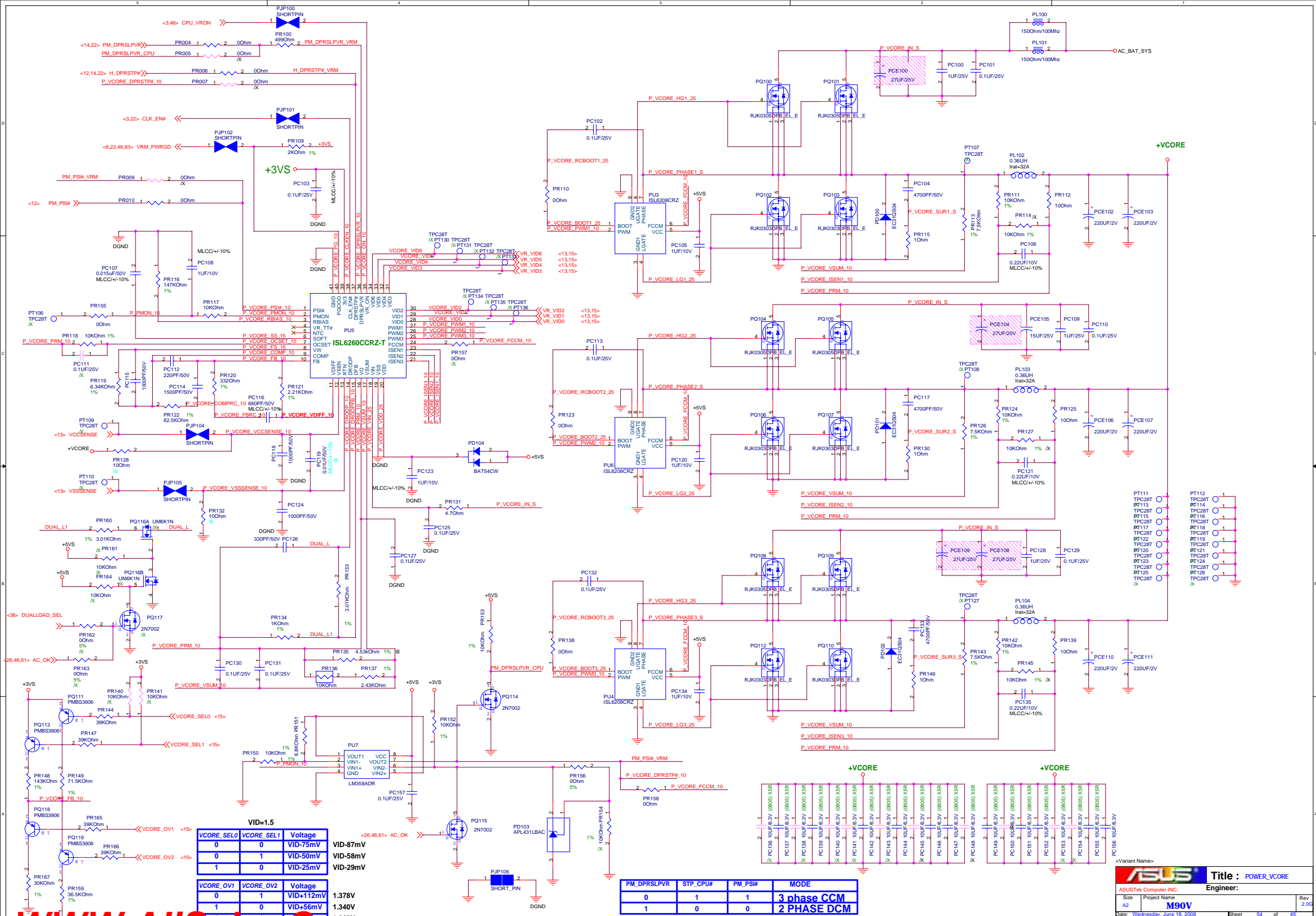


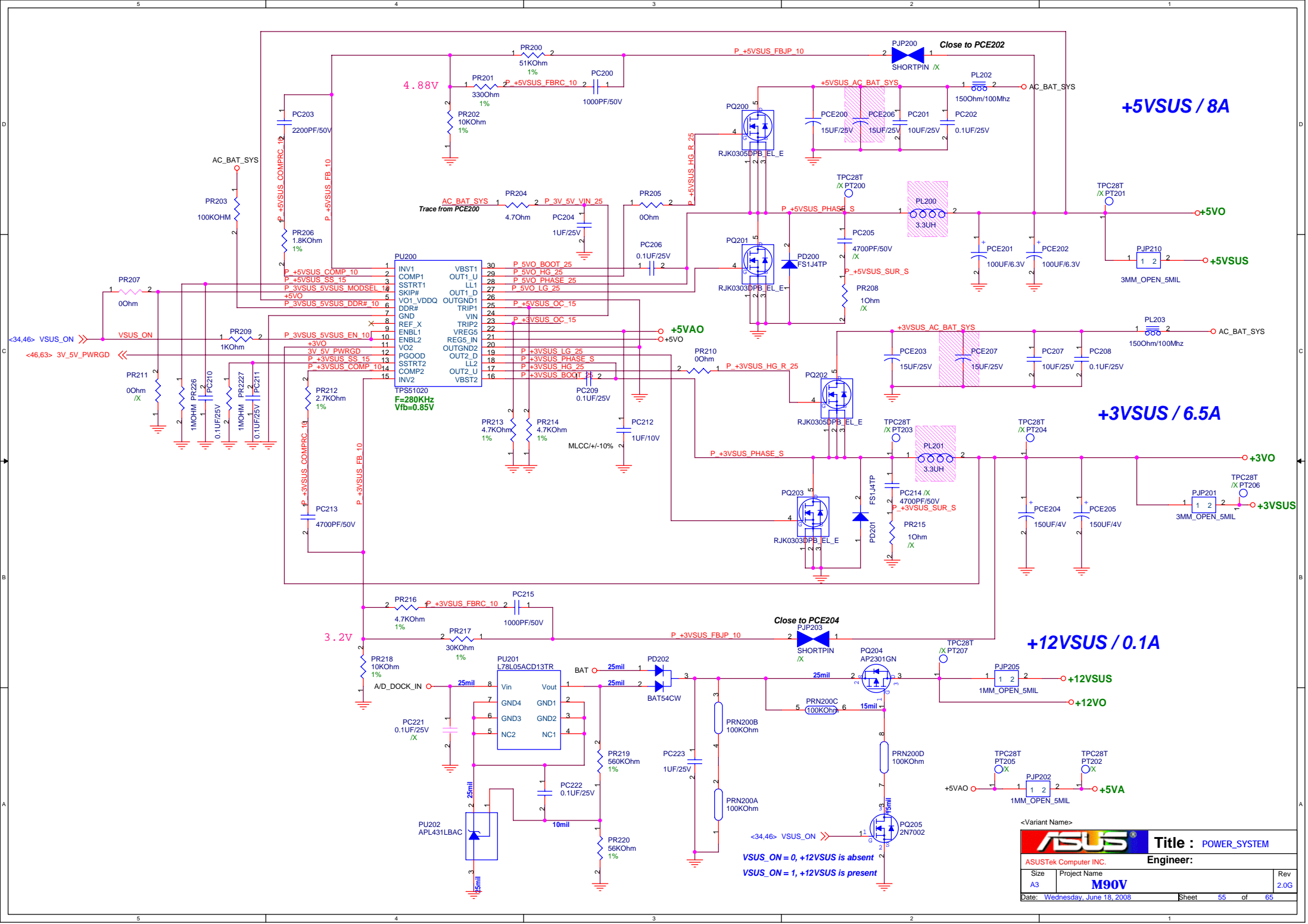
BAT-IN Connector

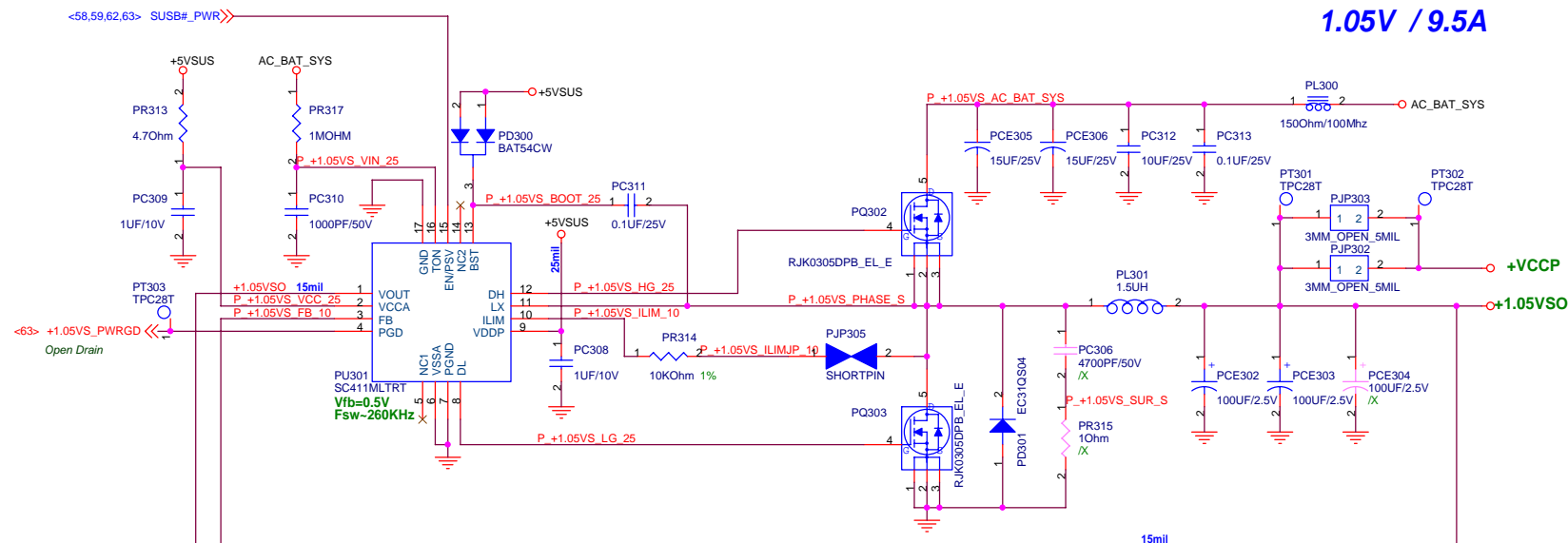








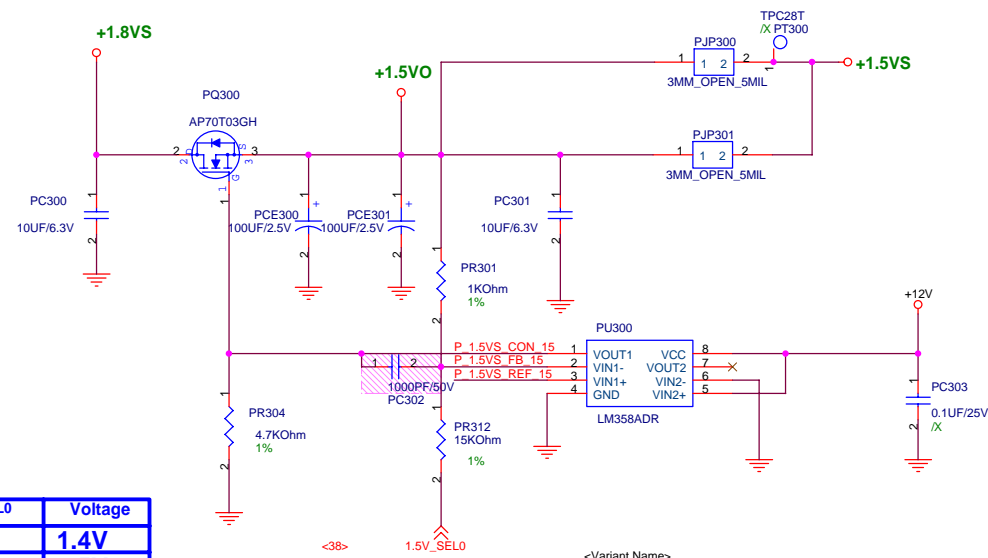




1.05V / 9.5A

+1.5V0 / 3A

for NB, SB, CPU VCCA



1.5_SEL0	Voltage
X	1.4V
L	1.5V

<Variant Name>

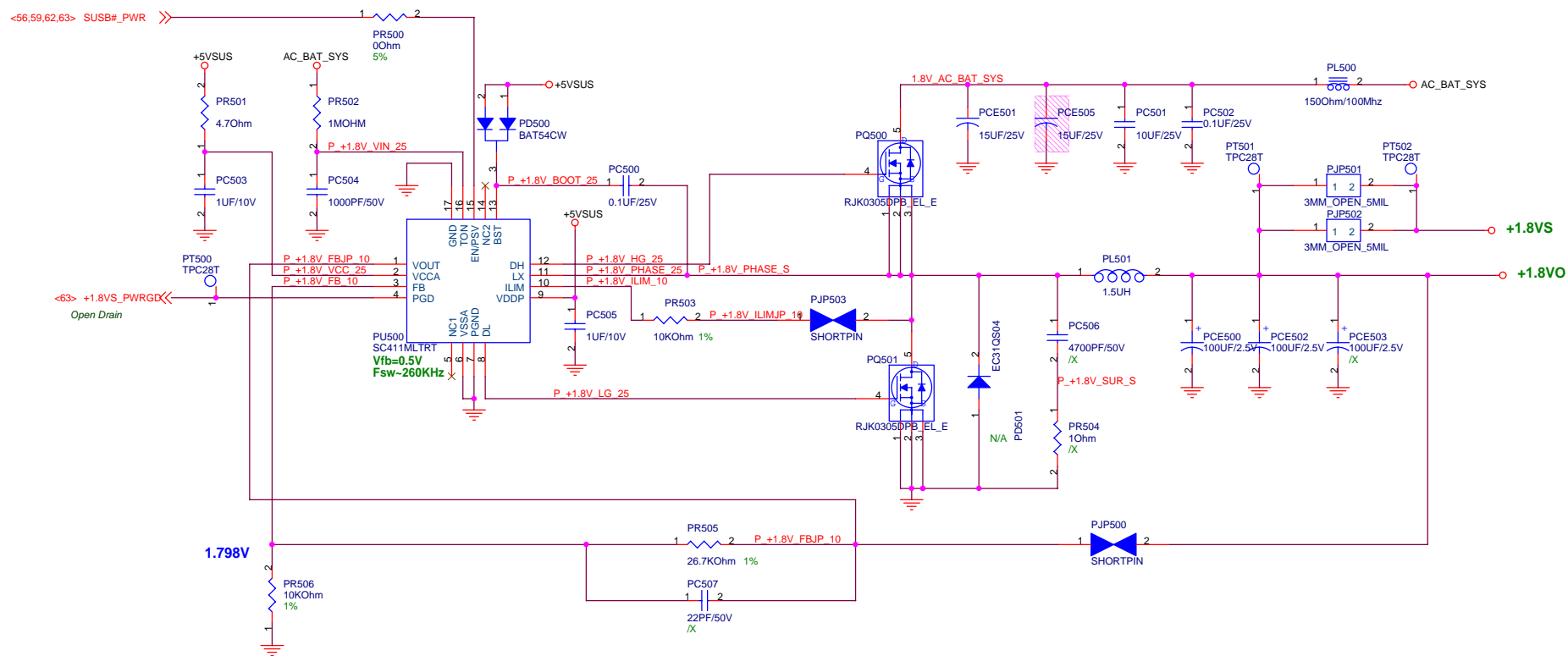
ASUS Title: POWER 1.5VS & 1.1VS & 2.5VS

<OrigName> Engineer:

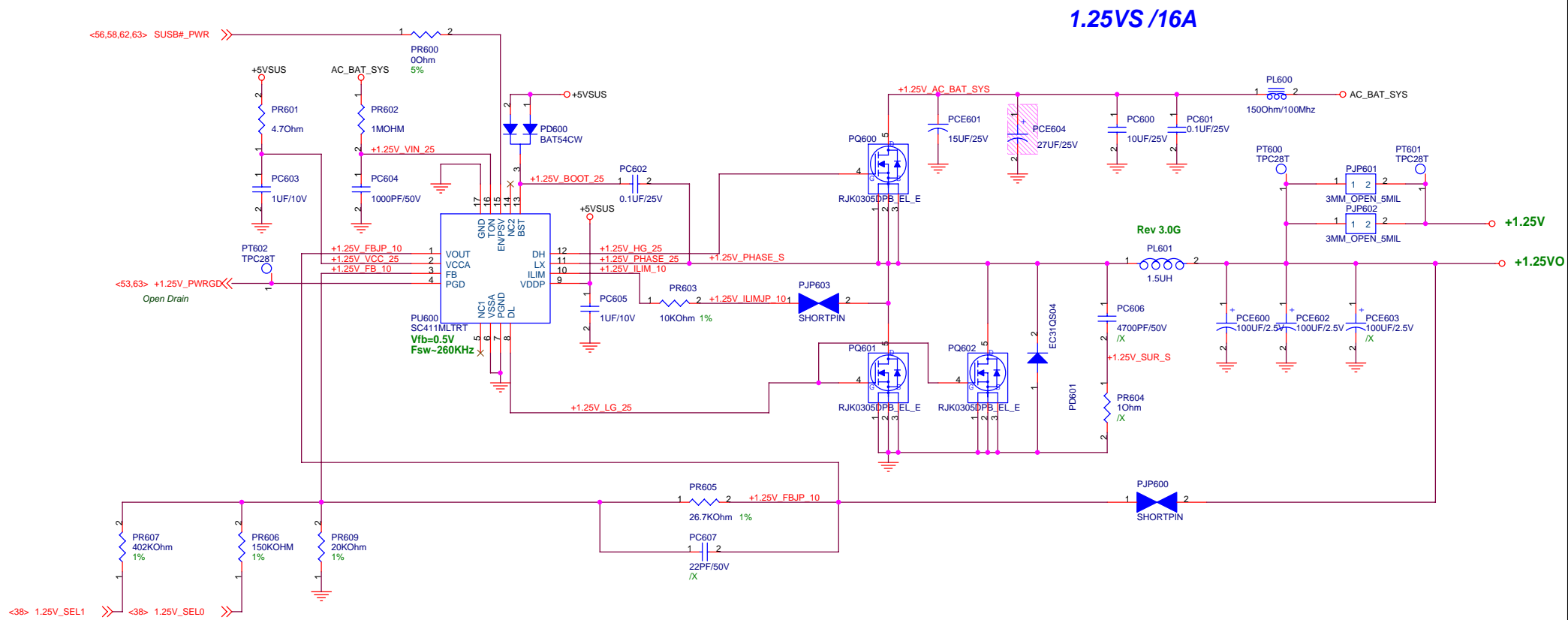
Size Project Name Rev

A3 M90V 2.0G

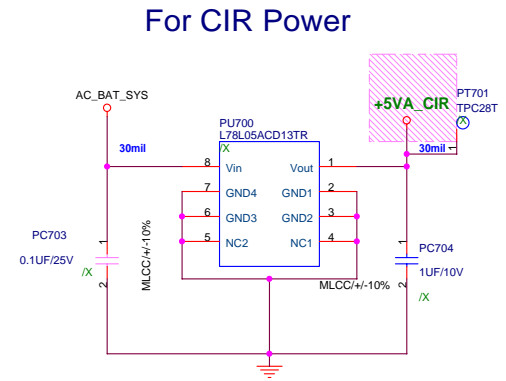
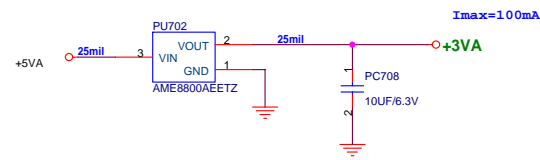
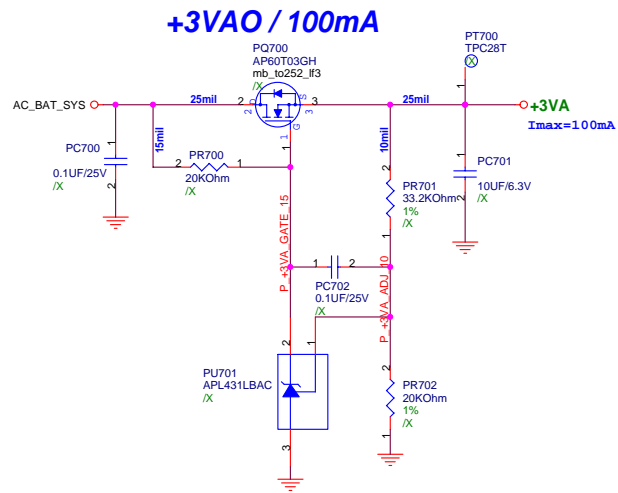
Date: Wednesday, June 16, 2005 Sheet 56 of 65



The schematic diagram illustrates a +2.5V 2A power supply circuit. The circuit is powered by a +3V input and a +2.5V input (labeled +2.5VS and Imax=2A). It features a voltage doubler stage using two TPC28T /X PT503 capacitors to generate +2.5VS. This is followed by a voltage divider using two TPC28T /X PT505 capacitors to produce +2.5V. The +2.5V is then regulated by a PU501 LDO (CM8562PG18) with a 100uF/6.3V capacitor (PCE504) on the input and a 100uF/6.3V capacitor (PC508) on the output. The output is further filtered by a 100uF/6.3V capacitor (PC509) and a 1000pF/50V capacitor (PC510). A 10Kohm resistor (PR507) and a diode (PU502 H431BN) are used for protection. The final output is +2.5V, labeled P +2.5V_REF_20.



1.25V_SEL1	1.25V_SEL0	Voltage
X	X	1.14
X	L	1.17
L	X	1.23
L	L	1.263



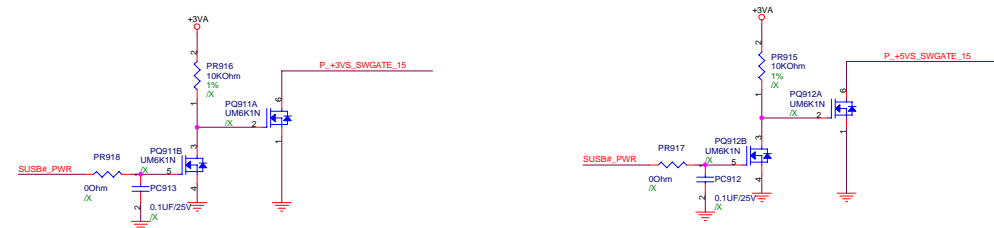
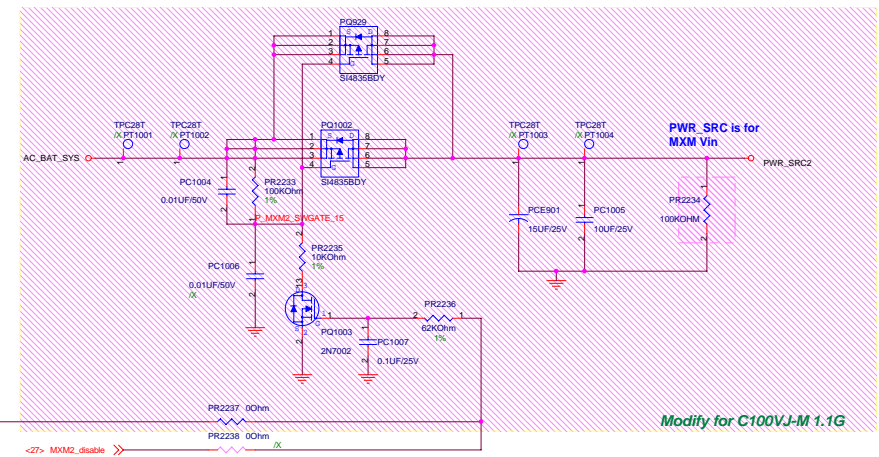
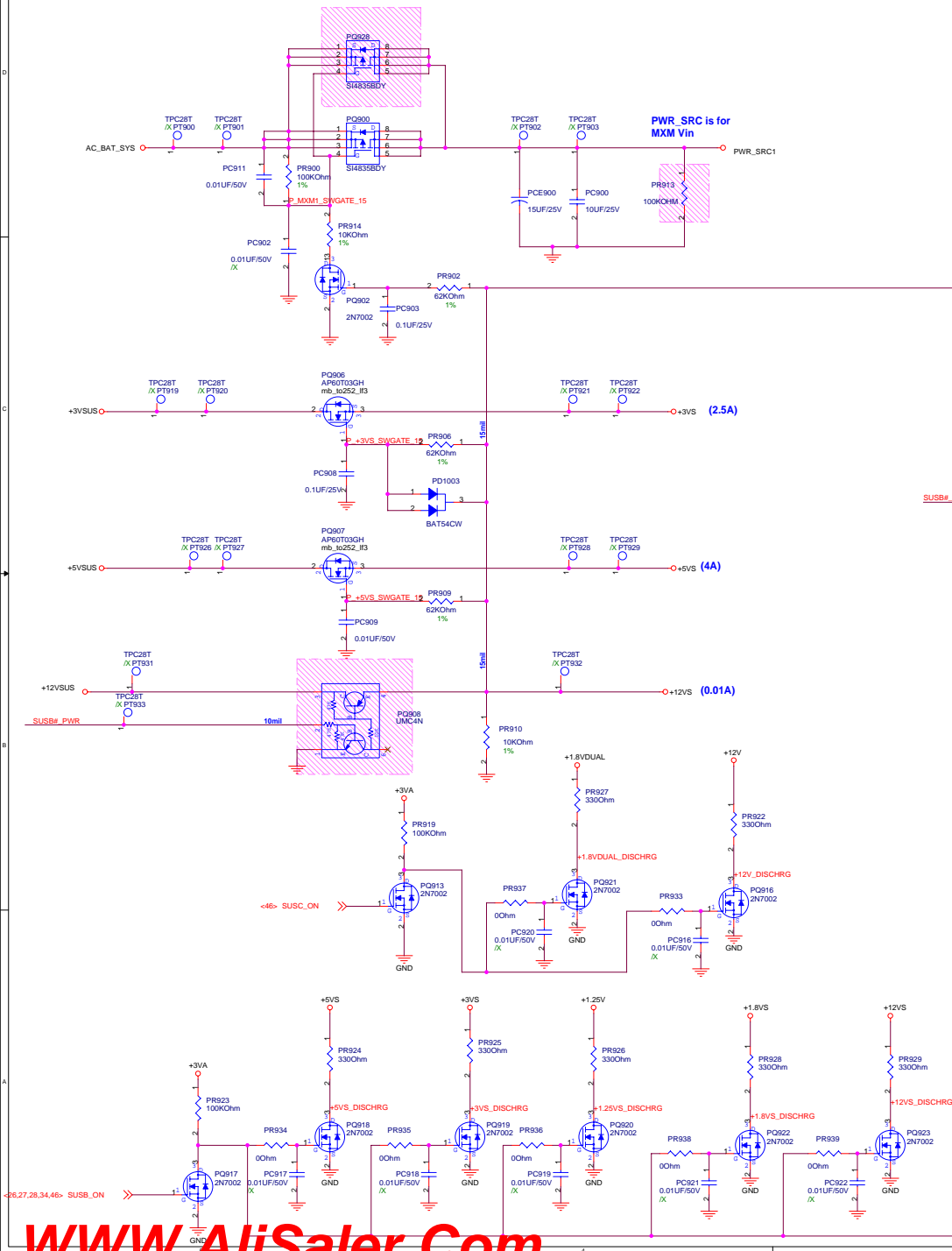
AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Adaptor Max. Current :

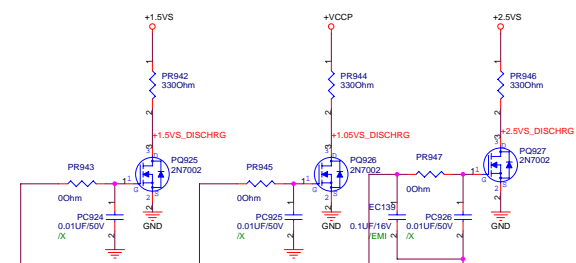
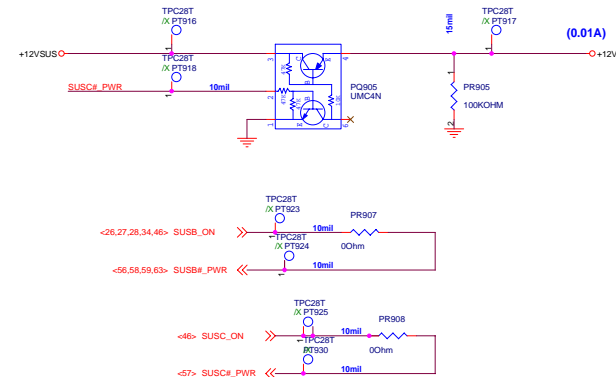
Mode pin : Vmode > 2.8V (try to LDO pin) ----> 4 Cells
2.0 > Vmode > 1.6V (floating) ----> 3 Cells
0.8 > Vmode (try to GND) ----> Learning mode
VICTL < 0.8V or DCIN < 7V --> Charger Disable

BAT_LEARN = 1, Battery discharges
BAT_LEARN = 0, charging voltage with 3 time VCTL (3 Cells)

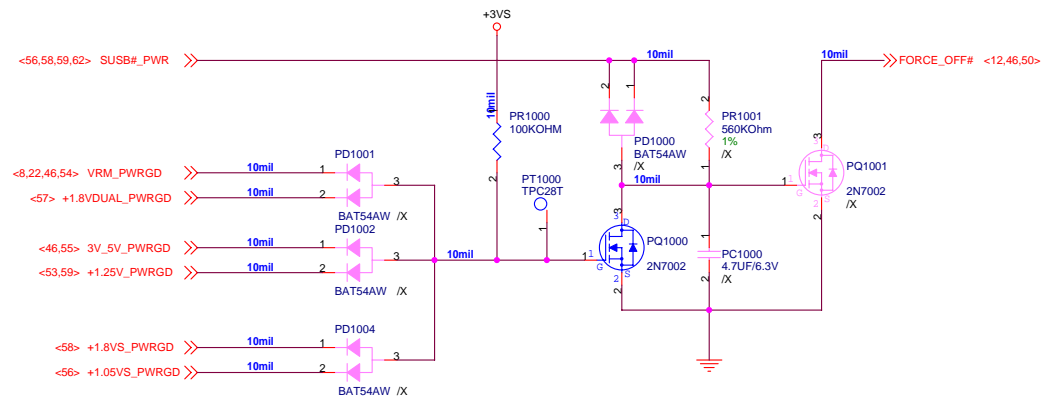
SUSB#_PWR POWER



SUSC#_PWR POWER



Power Good Detector



8/10
1. Change new power circuit from P53 to P62
2. Use single ESATA to replace the combination of ESATA and USB port (P38)
3. Add button, inverter and camera boards (P32)

8/13
1. Add Robson function (P37)
2. Remove LED (P50)
3. Because use SATA ODD(audio is digitsal signal), delete Audio analog single pin (P42)

8/15
1. Change DDR3 SO-Dimm; DIMM1 H4, DIMM2 H8,DIMM3 H12(P16~P18)
2. Add USB port (P32)
3. Change LVDS connector to 17" panel

8/16
1. Change MXM1 and MXM2 connectors to H16 (P25, P26)

8/20
1. MXM data pin change back to standard (P6, P8)
2. Change DC_IN jack
3. Change DDR3 Dimm3 to H8 temporary

8/21
1. Clock Gen. 3VA reserve (P3)
2. USB change to dual in one connector (P32)

8/22
1. Add VGA Fan control pin and change Fan voltage from +12VS to +5VS (P49)
2. Add ESATA voltage ESATA+1.8VS (P39)
3. Add for ESATA+1.8V power (P40)

8/23
1. Change RJ11-45 Conn. (P42)
2. change 1394 Conn. (P48)

8/28
1. Add LED control (P14)

8/29
1. Add LC FILTER==>VCCAPLL_EXP and VCCAPLL_EXP2 (P9)
2. VCC_EXT_PLL pin change to +1.25V

9/4
1. Reserve CAP (P10)(P15)(P18)
2. Add couple CAP (P32)
3. Add RC filter (P39)

9/6
1. Reserve GPIO Res for another control method (P39)
2. Change 2N7002 to SI3456BDV for power consumption
3. Add CPU frequency control (P47)
4. Add GPIO for VGA and System fan control (P47)
5. Add detection of MXM present pin (P47)
6. Add wireless lan LED control (P47)
7. modify fan control method and reserve +5V and +12V fan type

10/31
1. clock GEN change to 928 (P3)
2. change battery hold (P21)
3. Add audio singnal on MDC device (P22)
4. Move SATA ODD to port SATA4 and pull low the interlock switch (P23)
5. Remove S-singal pin on MXM (P26)
6. Change net name from SPDIF_OUT to HDMI_Aout(P26)
7. Modify USB circuit for different side application (P32)
8. Set E-SATA+1.8VS to /X on regulator side (P39)
9. Change ALC883 to ALC888S (P42)
10. Add audio AMP on SURR, Center and Woofer (P43)
11. Modify FAN control on MOSFET switch (P49)

11/1
1. DDR3 change to reverse type

